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1 Introduction

This report summarizes the design flows that currently exist for the research topics that are conducted in the individual ESR projects. This state-of-the-art overview is summarized per ESR project in Section 2. Based on this input, requirements for a joint, multi-disciplinary design flow are defined in Section 3. The requirements as well as state-of-the-art design flows will be used in deliverable D2.2 to define the design flow for the MyWave project.

2 Existing design flows

2.1 System Architecture and Development of RF Synchronization Concepts

In order to make the concept of massive MIMO truly distributive in nature, it is essential to allow large groups of neighboring nodes to form virtual antenna arrays for both transmission and reception. But to bring this concept from theory to practice requires the concept of synchronization to be applied at multiple levels in a distributive network. Broadly it is classified into two main categories. One to have phase coherency between multiple transceivers on a single node to achieve maximum benefit of transmit diversity and beamforming in phase arrays i.e. signals feeding into the transceiver units of each of the tiles should be both frequency and phase coherent. While second aspect deals with achieving frequency and time synchronization between the frontends that are distributed in a cell.

From implementation point of view, two fundamental challenges are as follows;

- To make transceiver units frequency and phase coherent despite random phase noise and parasitic that become more critical at mm-wave operation.
- Efficient calibration algorithms to synchronize distributive nodes in frequency, time and phase without constraining data throughput of network.

The concept of synchronization "between nodes" work on the basic principle of having all nodes agree on the same message, transmitting at the same time, same carrier frequency and to also control their phases for constructive combination at user terminal. Each node has independent local oscillator and therefore frequency variations must be corrected against signals drifting out of alignment during transmission. Frequency synchronization uses Master-Slave approach in which either user terminal or one mode broadcasts a carrier frequency allowing others to synchronize to it via operations performed in DSP. Phase synchronization is essential as each node has an ambiguous phase offset which becomes a part of channel estimation process and degrades channel phase information since it cannot be disambiguated from relative phase offsets. Timing synchronization deals with same symbol transmission at same time which if not maintained can cause inter-symbol interference. However, compared to carrier phase synchronization timing synchronization is a not a fundamental bottleneck, and there are multiple algorithms that can tackle timing synchronization for low and high data rates. [1],[2]

Whereas the concept of synchronization "within a node" involves achieving synchronization in terms of frequency and phase between several of the tiles (where each of the tiles host a number of on-chip

transceivers and local oscillator architecture usually implemented as phase locked loop) on a single node which if left unattended can prove to have disastrous affects for phased array performance of network. [3], [4]. The approach usually adopted is to make use of some calibration mechanism that tends to remove phase offsets between the transceivers of each channel periodically in order to make them more coherent.

However, the synchronization process for local oscillators is complicated by the fact that it involves two fundamental problems of phase noise and LO drift as function of temperature & time. Both issues are random with respect to time and cannot be calibrated out. In such an instance two obvious choices would be to either

 Reduce phase noise and LO drift to such an extent that channel-to-channel variation does not remain a bottleneck.

OR

• To design a LO sharing architecture such that channels become coherent despite the variations

The figure below summarizes the design flow of this project



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2.2 Power amplifier and antenna co-design strategy for optimised efficiency

For the development of 5G systems, the multi-physics analysis is carried out. The electrical, thermal and mechanical requirements are more important in multi-beamforming and massive MIMO systems as the overall performance of a transmitter depends heavily on the power amplifiers. The amplifiers are less efficient at mm-wave frequencies, the cooling systems are a crucial part of the design of the base stations. Requirements must be fulfilled at different levels such as transistor, layout, packaging and system. The performance of each level depends on the accuracy of the simulations. Therefore, the CAD software must be able to provide a result close to the intended implementation. The table below provides a summary of the necessary design parameters the CAD tool(s) must provide.

Design level	Description		
Schematic	Architecture: Class B, Balanced, Doherty Amplifiers.		
Electromagnetic	Layout: Transmission lines, Bias and Matching Networks.		
Parasitics	Packaging: Bottleneck on IC design, QFN, PQFN, etc.		
Heat Loss	Thermal analysis: Dissipation, Heat Flux, material dilatation.		
Stress	Mechanical analysis: Lifetime, Mechanical Breakdown, Vibrations.		

Table 1. Overvie	w of design	n parameters in	multi-physics	PA design.
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Transistor-Circuit Electrothermal Design Flow



Requirements:

• Thermal model based on 3D Finite-Element analysis

- Validation of the analysis by different electrical measurements on HBT (V_{be}, H₁₁, H₁₂)
- Validation on GaN HEMTs (Ron, 3ω₀)



Electro-Thermal-Mechanical Design Flow for Cooling Electronics

Requirements:

- Electrical, thermal and mechanical accurate models from circuit and material
- Library functions for CAD simulations
- Iterative Loops for equation solutions

Packaging Design Flow



Requirements for Packaging and System-Integration:

1) Performance requirements

- a. High-Q Passives for Co-Design of Active Front-End Components
- b. High-Gain Antennas
- c. Intra-System EMC
- d. Signal Integrity
- e. Power Integrity
- f. Heterogenous Integration
- 2) Reliability
- 3) Miniaturization
- 4) Cost

References:

[1] C. Fager, K. Andersson, P. Melin, M. Caruso, Y. Aslan, D. Prestaux, I. Ndip, M. Thorsell, E. Leclerc, V. Poisson, R. Sommet, "Integration and multi-physics challenges in 5G mm-wave system design", 49th European Microwave Conference, Paris 2019, Workshop.

2.3 Reconfigurable active-antenna array architectures for mobile users in mm-wave communications

At 20-60 GHz mm-wave band, the state-of-art design flows mainly include:

- a) Antenna in Package: choose on-substrate (PCB, LTCC, HDI, quartz glass) antenna/array topology; design transition layout to IC board (direct feeding pins, ball-grid arrays (BGAs), coupling apertures, waveguide interfaces) [1];
- b) IC distribution at RF (4 to 8-element TRX RFIC phased arrays to a single I/O port), or distribution at a lower frequency LO and IF (16- to 32-element TRX RFIC phased arrays are integrated with up-/down-conversion and PLL circuits)

Due to high loss and non-scalability, at W-band (75-110 GHz) or higher frequency, multi-physics and multiscale design flow for modeling and product development of highly integrated distributed MIMO systems at mm-waves that include active electronics, antennas and thermal management are not available in an integrated and logical flow.

Here are some existing state-of-art designs, but not logically coherent for a system design:

- a) 1D beam steering, full metal large array at 300GHz: fabricated by silicon-micromachining, fed by quasi-optical waveguides, frequency steering; [1]
- b) Fit the ICs in the area occupied by the N antenna elements: use dummy antenna elements to accommodate the dual-polarized TRx IC at 94 GHz; [3]
- c) Gap waveguide array + MMIC system design for point-to-point wireless link applications at 84GHz band: slot antennas in GWG structures for high efficiency, waveguide – microstrip line transition, MMIC control board.

For this project, a new multi-physics design flow for the co-design of active integrated circuits, antennas, and passive components of micro-electromechanical systems components (e.g. phased shifters, switches) is needed. Aiming at W-band and higher, large 2D phased arrays of our project are designed using metal

gap waveguide arrays: the first-dimension beam steering is realized by sub array modularization, the second-dimension beam steering is realized by integrating active phase shifters within antenna units:

1) Design high gain/efficiency antenna unit & array, available for integrated active components for large angle beamforming.

Choose antenna topology and simulate antenna unit cell & 1D array in E/H plane; fabricate & measure the 1D array to verify its beamforming performances; simulate sub array + feeding structure;

- Design active phase shifters & integration methods; simulate active phase shifter circuits; simulate integrated active antenna unit cell & sub array; fabricate & measure active sub array + feeding structure;
- Design low loss transition/layout between MMIC and antenna sub arrays. Simulate & fabricate B2B transition;
- 4) Check the whole system performances.
 fabricate & measure active sub array + feeding structure + transition + MMIC board;



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- [2] A. Gomez-Torrent et al., "A Low-Profile and High-Gain Frequency Beam Steering Subterahertz Antenna Enabled by Silicon Micromachining," in IEEE Transactions on Antennas and Propagation, vol. 68, no. 2, pp. 672-682, Feb. 2020, doi: 10.1109/TAP.2019.2943328.
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2.4 Strategies for energy-efficient high EIRP generation in mm-wave wireless radio links

The essence of 5G wireless networks lies in exploiting the unused high-frequency mm-wave spectrum ranging from 30 to 300 GHz. On the other hand, the multiple-input multiple-output (MIMO) technology is considered as one of the promising ways to improve spectral efficiency. Besides, massive MIMO is essential for mm-wave frequencies because it exploits beamforming gain for obtaining sufficient signal-to-noise-ratio (SNR) by combating high path losses. These kinds of systems have been developed in recent years.

In [1], fully digital beamforming (DBF) based massive MIMO transceiver has been designed. The first step in the design has already been established, which is to determine the beamforming architecture to employ. In this case, a DBF was selected. Secondly, basic system requirements were listed: operation band, signal bandwidth, maximum linear transmit power, cell coverage range, the data rate per single-user, the peak data rate for multiple users, and the highest modulation scheme supported. To meet the required system performance and coverage, some mm-wave design specifications need to be satisfied to ensure the signalto-noise-interference-plus-noise ratio (SINR). The total SINR is mainly contributed by the receive signalto-noise ratio (SNR) of the wireless link, local oscillator (LO) phase noise, modulation quality, and multiuser interference. From this analysis can be determined the array gain and the total transmitted power. The MIMO channel matrix is determined and, with it, the number of spatial multiplexing streams. These requirements are the input to design the elemental transceiver components such as front ends, the antenna element, antenna architecture, the IF transceiver, and the LO subsystem. The measurements of the proposed DBF-based massive MIMO transceiver are composed of two parts: the first is an RF performance of the transceiver, and the second part is an over-the-air (OTA) performance tests of the whole transceiver. Several beamforming systems have been described in [2]-[6] with almost the same design flow as the system described above.

Since the design of these systems entails the design of RF chains, channel estimation, design of antenna arrays; therefore, it is a multi-disciplinary effort. This project is focused on hybrid digital and analog beamforming systems focused on the development and optimization of algorithms for channel estimation and the design of antenna arrays. In figure 1, a design flow of an array antenna for hybrid beamforming applications is illustrated.

Requirements for MyWave multi-physics design flow

- With the continuing downscaling in feature sizes and increase of input power and operating frequency of high-density ICs and antenna arrays have led to extensive joule heating. This electromagnetic induced heat generating and resulting elevated temperatures adversely affect the performance and reliability of the devices. It is important to consider the reciprocal interaction between electromagnetic, mechanical and thermal aspects.
- Modeling these beamforming algorithms in the context of an entire system, including RF, antenna, and signal processing components, can help verify design choices at the earliest phases of the project and reduce the associated challenges.
- Design of front ends for beamforming applications.



Figure 1. Design flow of an antenna array.

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2.5 Energy-efficient and low-cost active front-ends for DM-MIMO

Fig. 2.6.1. demonstrates the possible scenario for connecting ideas from different research areas. The main idea of this design flow is that the specifications for each research are defined based on the requirements for the whole system, and not separately. At the same time, this system can be still somewhat modified depending on research results, however, the connection between all the topics can be made easier if there is some initial vision of general idea for certain DM MIMO system.

Another important feature is to have several intermediate stages of collecting the current results from each research area in order to understand and discuss the resulting theoretical system and to compare it to the one planned at the very beginning. These stages are included into the proposed design flow as "Common solution". According to this flow, each area have to make necessary modifications and then to continue research. This approach could make the whole project more efficient, since each researcher would take into account the requirements of other areas.



Fig. 2.6.1. Possible design flow for MyWave project

2.6 Analogue Radio-over-Fibre-fed antennas for massive deployment

The goal of the project is to design the receiver module with low noise level for "User – Base station" scenario. The module includes co-design of an antenna and a Low-Noise Amplifier (LNA).

The basic Idea of this design illustrated in Figure 1. The output impedance of the input matching network from final amplifier version will be used as optimal antenna input impedance for the best gain and noise system performance. In this way, the transformation to 50 Ohm between antenna and amplifier will become obsolete, resulting in the lowest loss and, hence, improved noise figure of the system.



Fig. 1. Illustration of the optimal antenna impedance for an LNA.

Currently anticipated design flow:

- 1. Low Noise Amplifier design and manufacturing of amplifier and amplifier parts separately (input and output matching networks, amplifier body).
- 2. Measurement and characterization of all components of an amplifier and amplifier in general.
- 3. Antenna design process.
- 4. Antenna manufacturing and measurement procedures
- 5. Design of the receiver module (antenna + amplifier) in the package.
- 6. Receiver module measurements.

2.7 Co-optimised antenna-circuit module integrating contactless interconnects

Today's vision on the next generation wireless networks is tightly connected to the concept of massive Multiple-Input-Multiple-Output (MIMO) systems. It is predicted that more than a hundred and up to a thousand antenna elements will be used in a single remote head after the year 2030 [1]. For such massive systems, next level of integration between antenna elements and power amplifiers must be achieved as the constrains on power efficiency and cost effectiveness become as stringent as ever [2]. Doherty power amplifier (DPA) scheme is considered by many a preferred PA scheme due it's high performance in a broader range of output powers [3]. The first integration step away from the conventional power combining networks and towards low interconnection losses was to match both main and auxiliary amplifiers of a DPA directly to two spatially separated antenna elements [4]. The next step would be to match a DPA directly to a single antenna.



Figure 2. Evolution of the antenna-PA integrations concepts (from [5]).

This way, antenna and PA circuit must be co-designed, and the characterization of the final device is complicated by the fact that the antenna is no longer a passive element. The design workflow for P8 will be based on the ESR's research group previous experience on the topic [5]. A DPA is designed first and the optimal load is calculated. Two-port antenna is then designed to have its impedance close to the optimal DPA load impedance. The antenna impedance is inserted into the circuit simulator as the DPA load impedance, gain and efficiency of the amplifier are evaluated. RF currents at the output of the amplifier are then used in the 3D EM solver as the antenna excitation. Performance of the device is evaluated in the anechoic and reverberation chambers.



Figure 3. Workflow of the integrated antenna-DPA design from [5]

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2.8 Highly efficient digital amplifier architecture based on GaN technology

Switch-mode power amplifier concepts have so far been considered for advanced amplifier concepts at frequencies below 3 GHz. At mm-waves, classical power technologies did so far not provide sufficient robustness to achieve high-switching speed while maintaining high power output. Nowadays most advanced GaN semiconductor technologies do allow to create high power levels at mm-wave clock speeds. Thus, new circuit design concepts are required at mm-waves to create new amplifiers for array concepts and to create efficient digital-switch structures for efficiently creating RF power and enhancing overall efficiency.

Presently, as a baseline, the design flow for a classical MMIC process would be the flow of a classical group III-V MMICs and is as follows:

1. The fabrication process for implementing the circuit is selected. This limits the components to those that can be realized using the relevant technology. A process design kit (PDK) is chosen and the models are verified in comparison to measurements from relevant hardware samples.

2. The actual circuit is designed using component libraries for active and passive devices from the PDKs on schematic level. Depending on the circuit, there are a wide variety of possible solutions, e.g. analysis of power amplifier circuit in the time domain for digital circuits or in the frequency domain using X- or S-parameters, or using the harmonic balance method. This mixture for mixed-mode digital circuit design is not yet established for the mm-wave frequencies and requires investigations.

3. Optimization of the circuit parameters such as output power, gain, efficiency is performed in order to find the best possible approximation for the required circuit properties.

4. Stability analysis is performed to ensure microwave stability for the multistage design.

5. Since parameter variances occur due to variations in the manufacturing process, their influence on the properties of the overall circuit must be investigated using sensitivity analysis. Depending on the required yield, it might be necessary to modify the circuit.

6. Finally, the circuit is transformed into a corresponding layout, either by automatic functions such autolayout functions from the PDK or by individual layout.

7. Using additional Electro-magnetic simulations this layout is verified and compared to the original electrical simulations. This process is repeated until the layout is also verified.

8. This resulting layout file is, after design rule check (DRC) and LVS (layer vs Schematic cross checks) used in most cases to directly produce the lithographic masks. If problems occur during the dimensioning process (e.g. a capacitor area that cannot be implemented due to its size), the design must be modified accordingly.

9. For antenna module design, additional check can be implemented, such as: inclusion of the MMIC module transitions into step 7.), further standing wave ratio (VSWR) considerations during the step 5.

10. Sequentially, also the module design will be added, including the thermal considerations to keep the amplifier MMIC within the SOA (safe-operating area) during operation.

2.9 Efficient power combining of GaN mm-wave amplifiers

For radio links, the achievement of high power linear operation is required to achieve high data-rates at maximum power added efficiency. At mm-wave frequencies, classical power combining to achieve high EIRP and matching to a 50 Ohm antenna interface creates a lot of losses, which are prohibitive even for GaN. Thus, new design concepts are required at mm-waves to create efficient multi-chip structures that efficiently feed the power directly to a planar low-cost and low-loss PCB. In this way, significant linear power levels are achieved, which are way beyond today's linear power levels and without having to consider complex classical split-block approaches for waveguide combining.

The mm-wave MMIC Design flow includes:

1. The fabrication process for implementing the circuit is selected, either based on III-V devices or on SiGe HBTs. A process design kit (PDK) is chosen and the models are verified in comparison to measurements from relevant hardware samples.

2. The actual circuit is designed using component libraries for active and passive devices from the PDKs on schematic level. For a power amplifier, simulations are performed in the frequency domain using X- or S-parameters, or using the harmonic balance method supported by load-pull measurements.

3. Optimization of the circuit parameters such as output power, gain, efficiency, linear power, and power compression and linearity is performed in order to find the best possible approximation for the required circuit properties.

4. Stability analysis is performed to ensure microwave stability for the multistage design.

5. Since parameter variances occur due to variations in the manufacturing process, their influence on the properties of the overall circuit must be investigated using sensitivity analysis. Depending on the required yield, it might be necessary to modify the circuit.

6. Finally, the circuit is transformed into a corresponding layout, either by automatic functions such autolayout functions from the PDK or by individual layout.

7. Using additional electro-magnetic (EM) simulations this layout is verified and compared to the original electrical simulations. This process is repeated until the layout is also verified.

8. This resulting layout file is, after design rule check (DRC) and LVS (layer vs Schematic cross checks), used in most cases to directly produce the masks. If problems occur during the layout process, the design must be modified accordingly.

For antenna module design, additional checks can be implemented, such as: inclusion of the MMIC module transitions into step 7.), further standing wave ratio (VSWR) considerations during the step 5. Sequentially, also the module design will be added, including the thermal considerations to keep the amplifier MMIC within the SOA (safe-operating area) during operation. The split-block co-design is performed sequentially, in a similar way the split block can be replaced by QFN (quad-flad no lead) design. Further, the antenna co-design is added, again, sequentially.

2.10 Channel emulation platform for system testing mm-wave mobile user scenarios

Reverberation chambers attracted great attention from researchers and industry with the advent of 5G wireless communication. To emulate the real-life multipath channel characteristic, RF absorbing materials are elaborately placed in the reverberation chamber to introduce additional fading paths. However, one of the main drawbacks of loaded RC in the context of mm-Wave 5G communications is that directive effects are lost. Therefore, we aim to develop a chamber that can capture angular dependence and the dynamics of moving users. To this aim, we will study, design and develop a wall-tiling system that has the capability of switching the behavior of individual tiles from purely reflecting to purely absorbing, controlled by an electronic switch. As a first step, electrically controlled mechanical movement will be considered, and depending on the outcome followed by fully electronically reconfigurable tiles. This will give us the ability to both emulate directive and time-varying effects. The complete system will be designed and integrated in TUE's reverberation chamber, which will serve as the test platform for the distributed base-station system developed in MyWave.

As shown in the flow chart, to evaluate the performance of the loaded chamber the requirements and specification should be determined firstly. After designing the basic architecture, as a first step, electrically controlled mechanical movement will be considered. If this design can meet all the requirements or there is still very large room for improvement during the preliminary test this scheme is proven to be feasible. Otherwise, we will try another plan-fully electronically reconfigurable tiles loaded chamber if it can't pass the preliminary test and no room left for improvement. The alternative plan will also be validated via preliminary and integration test. Besides, repeated trial and error will be conducted which are denoted by the bent arrow line in red.



2.11 Energy efficient signal processing for DM-MIMO systems

In this project, strategies will be developed that make efficient communication possible. In principle, multiple orthogonal strategies have to be realized by the Remote Radio Heads (RRHs), one for each transmitting/receiving user. The RRH's act as relays between source or destination and the users. It is the objective of this project to design the signal processing algorithms and protocols for the small-scale Distributed Massive MIMO (DM-MIMO) test-bed of project P15. This project is based on multi-user information theory, more specifically broadcast, multiple-access and relay transmission protocols. To make transmission reliable, the application of coding techniques is crucial. The state-of-the-art flow chart of this project is shown in Fig. 1.



Figure 4: State-of-the-art design flow for project P13.

2.12 Digital array calibration techniques and synchronisation for DM-MIMO

Below figure provides a high-level block diagram that illustrates the operation of channel-reciprocity based MU-MIMO on the hardware, including UL channel training, DL MU-MIMO transmission, and the compensation mechanisms (synchronization and calibration) needed to enable such coherent DL MU-MIMO transmission. In the "CAL" block, the pre-coded signal at each AP is calibrated, which compensates for the nonreciprocal amplitude scaling and phase rotations introduced by the transmitter and receiver AP hardware. The action of synchronization blocks that indicated by "sync" and "SYNC" at the user terminal (UT) and AP side, respectively, are as follows. Synchronization at the UT side (both transmitter and receiver) and at the AP receiver takes care of frame and carrier frequency synchronization in order to transmit and receive on the assigned time slots and demodulate the OFDM signals with negligible intercarrier interference (ICI). In contrast, synchronization at the AP transmitter side plays a critical role in the

distributed MU-MIMO architecture, since it needs to compensate for timing misalignment and the relative phase rotation of the DL data blocks, transmitted simultaneously by the jointly pre-coded APs.



2.13 Digital Radio-over-Fibre for flexible mm-wave D-MIMO systems

Desing Flow for P15 has been shown by Figure 1. In the breif calarification, it is divided into Software Design Flow and Hardware Design Flow. Software Design Flow covers transmitter and receiver part, they follow more or less same steps. Start from specification, then, there should be parameter and structure of softeare for each part. In the simulation, some initial and basic issues could be revealed to improve software design. Co – simulation is helpful to see how transmitter and receiver match with each other in pure software environment. Implementation is key step to let software be runnable in real system. Co – varification is used to varify the possibility of software in system.

In the Hardware Design Flow, specificaiton introduce goals, properties and other details. Digital and Analog board have initial result through schematic and PCB design. Review and unit test is used to localize the sourse of potential problems. Standard design flow for antenna is consist of topology choice, design, simulation, review and test. Integration is second last step to integrate all parts and measurements give resonalbe resuts to finish our design.



Figure 5. Design Flow for P15

3 Requirements for MyWave multi-physics design flow

Based on the state-of-the-art design flows summarized in the preceding section, a number of requirements can be identified for a joint, multi-physics design flow for the MyWave project.

Requirement	Description
Software support: The design flow shall support the following software tools: Cadence Advanced design system CST MATLAB Quartus (or vivato)	Cadence and CST for layout, extraction of circuit parameter, evaluation of performance of IC. MATLAB and Advanced design system for system level simulations and/or algorithm development Both Cadence & CST are equally of importance since above 90 GHz there are lots of parasitic that cannot be extracted without full 3D EM simulation. Quartus (or vivato) is based on design specification, need FPGA platform to accelerate process.
The design flow shall support multiple design iterations	Multi-disciplinary designs require multiple design iterations on various levels. A first-time-right design does usually not exist.
The design flow shall support concurrent design tasks.	As 15 researchers have to work in parallel on different system aspects, the design flow must ensure coherence between the different design tracks.