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## Literature report on state-of-the-art mm-wave electronics
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## Contents



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# 1 Introduction

The use of millimeter-wave frequencies for communications brought several challenges for its system deployment. Large attenuation, demanding linearity and efficiency are just a few goal parameters to be enhanced in the design of power amplifier. The design of such modules involves not only a selection of material but also application-specific architectures. This report is organized as follows: In the first chapter, provides a compilation of state-of-the-art designs for the millimeter-wave power amplifiers. In the second chapter, the recent advances in power amplifiers (PA) design are presented to show what is currently available for antenna engineers. The third chapter will define the system architectures and will show the development of RF synchronization concepts. The last chapter is dedicated to architecture and technology choices for power-efficient-mm-Wave frontends.

# 2 State-of-the-art designs for the millimeter-wave power amplifiers

The two main branches of semiconductor materials are the metalloids and the III-V compounds. Silicon and Germanium are in this metalloid group, which are well known and widely studied materials for highly integrated systems such as microprocessors, providing low manufacturing cost in mass production. These are the major advantages in this material group. The III-V compounds are relatively new materials with Gallium-Arsenide, Gallium-Nitride and Indium-Phosphide as the key players. These compounds can reach comparable high frequency, high power and high thermal dissipation, but are not as good as Silicon in terms of integration. In Table 2.1, a summary of the semiconductor materials used for transistors in power amplifiers is shown.

| Material | Bandgap (eV) | Electron Mobility ($cm^2$/Vs) | Critical Field Ec (V/cm) | Thermal conductivity σT (W/m*K) |
|---|---|---|---|---|
| **Si** | 1.12, I | 1,400 | 300,000 | 130 |
| **Ge** | 0.661, I | 3,900 | 100,000 | 58 |
| **GaAs** | 1.424, D | 8,500 | 400,000 | 55 |
| **GaN** | 3.44, D | 1,500 | 3,000,000 | 110/200 |
| **InP** | 1.344, D | 5,400 | 500,00 | 68 |

Table 2.1. Semiconductor materials use for transistors in power amplifiers [1].

Figure 2.1 contains the information of the power vs frequency for power amplifiers with different materials, including the behavior of each one. In general, Gallium-Nitride offers the highest output power whereas the Indium-phosphide reaches the highest frequencies.

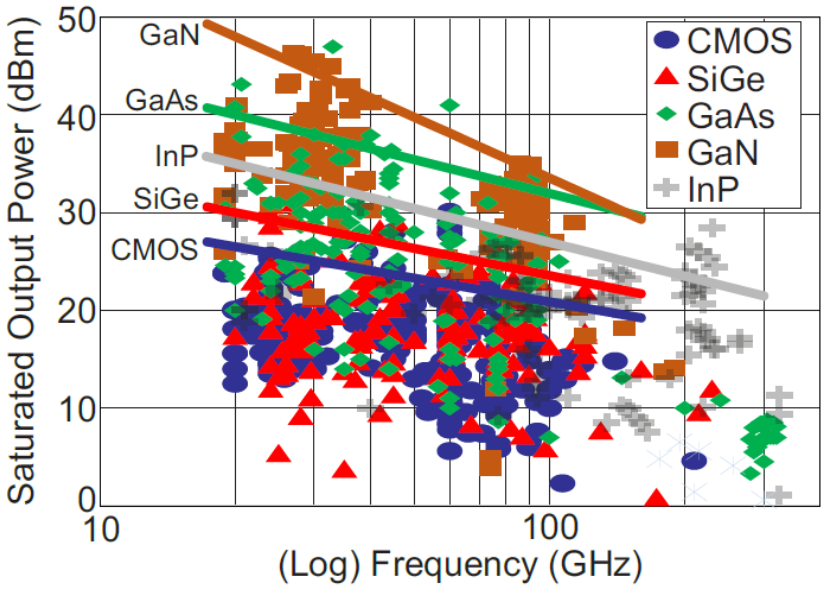


Figure 2.1: Technology performance [1].

In Figure 2.2, the most relevant structures for transistors and power amplifier design are sketched by the author's best knowledge. For silicon, the LDMOS offers a high performance in terms of power-handling, but only in the range of sub-6GHz frequencies. The major players above the 6GHz frequencies are the HEMT, HBT and BiCMOS, which differ in frequency range, output power and applications.

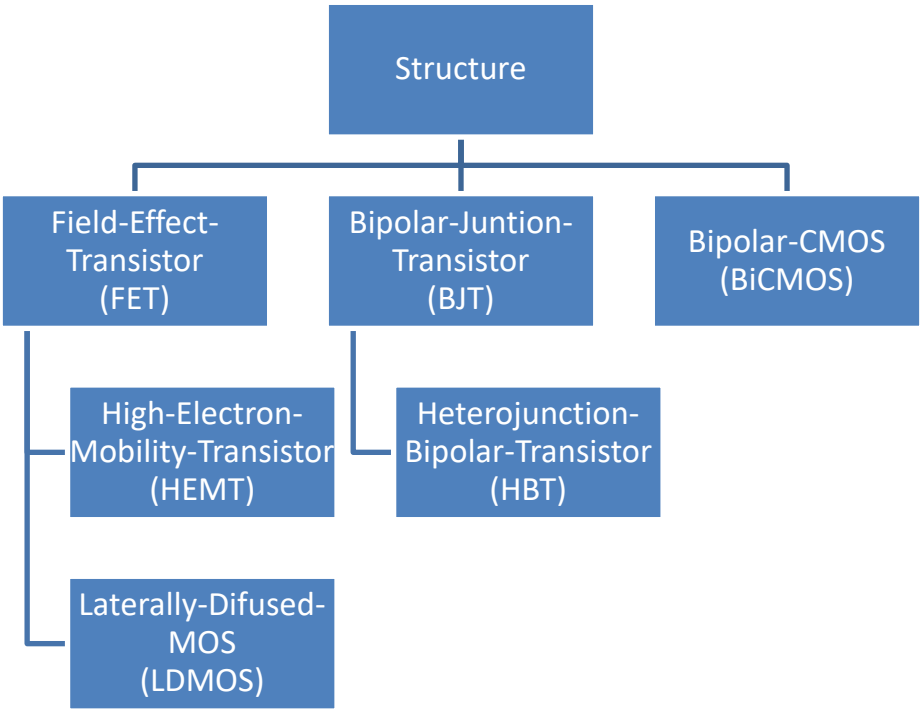


Figure 2.1: Common structures for transistors in the millimeter-wave ranges, sketched by the author's best knowledge.

## Architectures

Different architectures are available for power amplifier design, from single to multi transistor. Single transistor architectures heavily depend on the bias point, which can be swept to go from Class A amplifier to Class E. For high peak-to-average power ratio modulation schemes, the simple architectures do not satisfy the system requirements. Therefore, other topologies are studied in the millimeter-wave range, namely the Balanced, Doherty, Chireix, Distributed and Load-Modulated-Power-Amplifier. From this group, the Doherty, Chireix and Load-Modulated-Power-Amplifier are based on a technique called Load-Modulation, where the load is changed to change the impedance seen by the transistor and preserve a high efficiency. Until now, there is no Load-Modulated-Power-Amplifier or Chireix amplifier available in the millimeter-wave range. On the other hand, the Distributed and the Doherty power amplifiers are investigated [2] in this frequency range, as they offer broadband and high efficiency capabilities, respectively.

As a remark, it is of interest to study the effect of load variations to the performance of power amplifiers. The load variations are usually due to mismatch, beamforming and beam steering of antenna arrays. Highly sensitive amplifiers to this effect can have a reduction on their efficiency, linearity and output power as the optimal load connected to the power amplifier varies. This would be crucial in the millimeter wave range when beam steering is required due to the inherent high directivity of the signal.

In [2], a compressive review of the main solutions for the different mm-wave frequency bands is presented. This report is summarized as follow:

**K-bands (18-40 GHz)**

In this band, most of the publications report works in Gallium-Nitride or CMOS, which are the most promising technologies for this frequency range.

| REF | Year | Technology | Freq. (GHz) | Psat (dBm) | PAEsat (%) | SS Gain(dB) |
|---|---|---|---|---|---|---|
| **[3]** | 2015 | 200nm GaN/SiC HEMT | 26 – 30 | 45.5 | 32 | 22 |
| **[4]** | 2016 | 180nm SiGe HBT | 20 – 28 | 29.5 | 13 | - |
| **[5]** | 2016 | 28nm Bulk CMOS | 28 | 19.8 | 43 | 13.6 |
| **[6]** | 2018 | 100nm GaN/Si HEMT | 37 – 43 | 40 | 23 | 18 |
| **[7]** | 2018 | 130nm SiGe BiCMOS | 12 – 40 | 19 | 8 | - |
| **[8]** | 2018 | 90nm CMOS | 22 – 30 | 25 | 27 | 15 |
| **[9]** | 2019 | 100nm GaN/SiC HEMT | 26 – 35 | 37.8 | - | 22 |
| **[10]** | 2020 | 45nm CMOS SOI | 24 – 40 | 19 | 36.6 | 12 |

Table 2.2: Power Amplifiers topologies in the K-bands.

As presented in Table 2.2, the frequencies are overlapping in a few ranges. Also, the combining techniques and the number of stages can enhance the Psat and efficiency. There is also a recent effort to design Doherty amplifiers as reported in the following works summarized in Table 2.3.

| REF | Year | Technology | Freq. (GHz) | Psat (dBm) | PAEsat (%) | $PAE_{OBO}$(%) |
|---|---|---|---|---|---|---|
| **[11]** | 2019 | 150 nm GaAs pHEMTs | 26.5–29.5 | 25 | 35 | 25 |
| **[12]** | 2019 | 100 nm GaN/Si HEMT | 27.5–28.35 | 32 | 25 | 28 |
| **[13]** | 2019 | 45 nm CMOS SOI | 27 | 23.3 | 40.1 | 33.1 |
| **[14]** | 2019 | 130 nm SiGe BiCMOS | 29–31 | 16.8 | 20.3 | 13.9 |
| **[15]** | 2020 | 130 nm SiGe BiCMOS | 24–30 | 28 | 30 | 20 |

Table 2.3: Doherty Power Amplifiers designs in the K-bands.

**V-band (40-75 GHz)**

As the peak attenuation at 60GHz is high, the V band is mostly used for high data rate communication in short distances, for example, indoors such as WiFi and sensors. Table 2.4 reports the main works for power Amplifiers in the V-band.

| REF | Year | Technology | Freq. (GHz) | Psat (dBm) | PAEsat (%) | SS Gain(dB) |
|---|---|---|---|---|---|---|
| **[16]** | 2015 | 150 nm InP HEMT | 71 – 76 | 26 | 23 | 10 |
| **[17]** | 2016 | 90 nm SiGe | 68 – 91 | 27.3 | 12.4 | 19.3 |
| **[18]** | 2018 | 70 nm GaN HEMT | 70 – 86 | 30 | 8 | 16 |
| **[19]** | 2019 | 45 nm CMOS SOI | 56 – 63 | 28.5 | 15 | 24 |
| **[20]** | 2019 | 45 nm CMOS SOI | 60 | 20.1 | 26 | 13 |

Table 2.4: Power Amplifiers in the V-band.

As the attenuation in this band is relatively high, the frequency reuse concept for base stations is a possible suitable. In addition, the range 37-50 GHz is proposed for the next-generation communication for non-stationary satellite constellation.

**W-band (75-110 GHz)**

For this frequency range, the atmospheric attenuation is lower, but the multi-stage architectures are crucial. The frequency bandwidth is larger, and the efficiency decreases considerably. Table 2.5 reports the main works for power amplifier designs in the W-band.

| REF | Year | Technology | Freq. (GHz) | Psat (dBm) | PAEsat (%) | SS Gain(dB) |
|---|---|---|---|---|---|---|
| **[21]** | 2016 | 90 nm SiGe BiCMOS | 68 – 91 | 27.3 | 12.4 | 19.3 |
| **[22]** | 2016 | 100 nm GaN HEMT | 75 – 110 | 45.7 | - | 14 |
| **[23]** | 2017 | 250 nm InP DHBT | 93 | 12.4 | 41.7 | 10 |
| **[24]** | 2018 | 100 nm GaAs pHEMT | 92 – 102 | 27 | 12.5 | 27 |
| **[25]** | 2018 | 50 nm GaAs mHEMT | 65 – 125 | 22 | 10.7 | 16.8 |

Table 2.5: Power Amplifiers in the W-band.

In general, the HEMT (High Electron Mobility Transistors) technology can cover the whole range of frequencies from sub-6GHz to 110 GHz, but the other technologies and materials may offer better performance in terms of bandwidth or efficiency. From the technology perspective it is

possible to find transistors that operate in the ranges designated for 5G mobile communications, but new architectures can be proposed with optimized combiners for better efficiency, which are also less sensitive to the changing load conditions.

# 3 Recent advances in power amplifiers (PA)

One of the efforts for the next generation wireless communications is centered around developing a millimeter-wave integrated antenna-circuit module. Such module must include many radiating elements under the Multiple-Input-Multiple-Output (MIMO) design concept. Up to a hundred or more antenna elements might be needed (Massive MIMO). Power transfer to the antenna then becomes a big issue, as it becomes more and more inefficient as the frequency increases [26]. In this chapter, the recent advances in power amplifiers (PA) design are presented to show what is currently available for antenna engineers.

### Technology processes

Before starting the design of a microwave device, a choice of a fabrication technology must be made first. The four most popular picks today are HEMT in either GaAs or GaN, silicon Complimentary Metal-Oxide-Semiconductor (CMOS), Field Effect Transistors (FETs) or SiGe Heterojunction Bipolar Transistors (HBT). Table 3.1 contains a brief comparison of these technologies, more detailed comparison can be found in e.g. [27].

| Technology | Brief pros and cons description | Concerning antenna co-integration |
|---|---|---|
| **GaAs HEMT** | PAs with high output power and low noise. High cutoff frequency 400-500 GHz. Very popular choice for low-noise amplifiers, mixers and PAs. Relatively high cost. | Decent integration antenna-PA capabilities. Low substrate losses. Low thermal conductivity, heat dissipation problems when many PAs are very close to each other (low power density). |
| **GaN HEMT** | Highest breakdown voltages and output powers, up to 5 times that of GaAs. Wafers more expensive than GaAs. Lower cutoff frequency about 200GHz | Good thermal conductivity and high output powers makes it possible to efficiently combine many PAs on a smaller chip area. Not feasible for antenna-on-chip designs. Might not be effective when large antenna arrays are required |
| **CMOS** | The cheapest process, many commercial vendors available, low cost and high-volume production speeds up prototyping. Cutoff | Very good integration capabilities. High substrate losses in low-resistivity silicon. Low transistor breakdown voltage, not ideal if high |

| | | |
|---|---|---|
| | frequency higher than in GaN, but less than in GaAs. | EIRP (many antenna-PAs elements) is desired. |
| **SiGe HBT** | All the pros of CMOS, but the cutoff frequency is the highest of all above 500 GHz. | All the pros of CMOS, but PAs are much more suitable for the high-power amplification. |

Table 3.1. Main Transistor technologies.

Figure 3.1 is taken from [28] and shows a rough comparison of peak output power of the transistors superimposed over the estimated 5G system requirements.

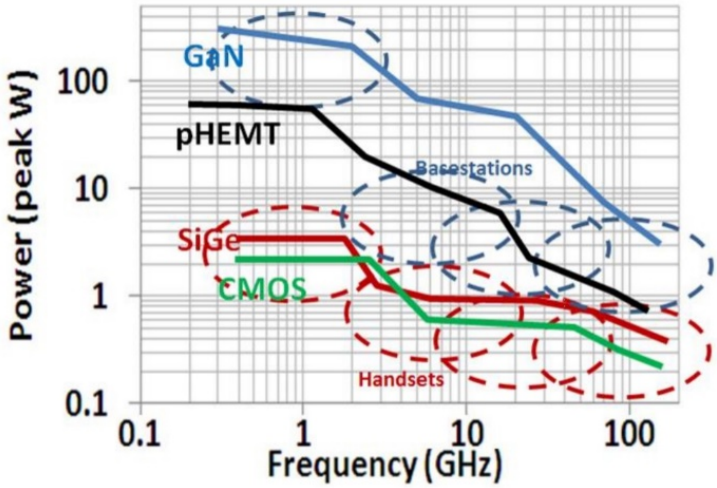


Figure 3.2: peak output power vs frequency for various device technologies based on latest demonstrated designs as of 2016 (solid lines), and estimated requirements for 5G power amplifiers (dashed). Taken from [28].

The data presented above aims to help to make a fair comparison between different PA designs. Even though GaN- and GaAs-based amplifiers exhibit better performance, CMOS and SiGe processes are non-less popular due to their advanced IC integration capabilities (c.f. [29]–[31]).

### Doherty Power Amplifier

The efficiency of the conventional power amplifiers peaks at certain input power level and drops down rapidly as the input power decreases. Due to the nature of signal processing protocols, the amplifiers are often forced to work at the powers below their peak efficiency levels (back-off power). In 5G networks, the efficiency of PAs at the back-off power levels may drop to as low as 2-5%. A Doherty Power Amplifier (DPA) combines class AB or class B amplifier with a class C amplifier to realize active load modulation. DPA thus takes the best from both PA classes and has an improved back-off efficiency. It has been one of the most popular PA choices for previous generations of networks [32] and now a lot of work is being done to implement DPA at above 30 GHz frequencies with the view to integrate it with antenna structures, e.g. in [33], where a successful power combining scheme from several DPAs at 60 GHz is described in great detail. It is worth mentioning that at Chalmers University of Technology – MyWave participating institution

– novel results on PA-antenna integration have recently been achieved [34]–[36]. A brief overview of the current state of the topic in CMOS/SOI can be found in [37].

Figure 3.2(a) shows the number of papers on PAs and DPAs versus year, [32]. Figure 3.2(b) shows a ratio between papers on DPAs and papers on PAs. The plot (c) shows a comparison between the normalized efficiency of a class B amplifier (in blue) and different DPA realizations (other colors).

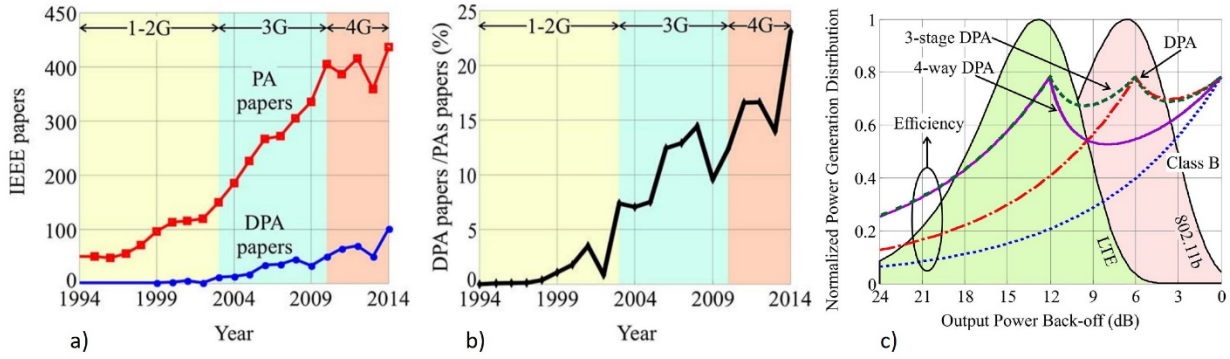


Figure 3.3.: Number papers on PAs and DPAs versus year (a), ratio between papers on DPAs and papers on PAs (b). The plot (c) shows a comparison between the normalized efficiency of a class B amplifier (in blue) and different DPA realizations (other colors). All plots are taken from [32].

## Power combining and antenna integration

Even though DPAs are more efficient than conventional PAs, power combining from several amplifiers to a single antenna element is still required in order to reach adequate EIRP (Equivalent Isotropic Radiated Power). [33] presents a good review of the recent advancements in power combining and multiport antenna feeding. In [38] researchers achieved very high EIRP by combining power from the total of 16 PAs into four ports of a slot antenna that is designed to operate around 60GHz. This and similar devices perform well in many regards, but they cannot be considered as elements of a massive array due to large interconnection losses in power combiners, and high-power consumption of each element due to 16 PAs at each antenna port. Regular PAs are used instead of DPAs because of the design issues and DPA instabilities that arise when trying to optimize several DPAs to feed one antenna element. Another class of solutions aims to reduce the interconnection losses via eliminating power combiners from the circuit. An example of this approach is the work carried out in [39], where both main and auxiliary amplifiers of a DPA each feeds an antenna element, and the mutual coupling between the antennas plays the role of active load modulation. It is thought now that the direct power combining at the antenna ports is the next integration step that can further reduce interconnection and matching losses (c.f. [40]). Figure 4.3 shows the evolution of DPA-antenna integration.

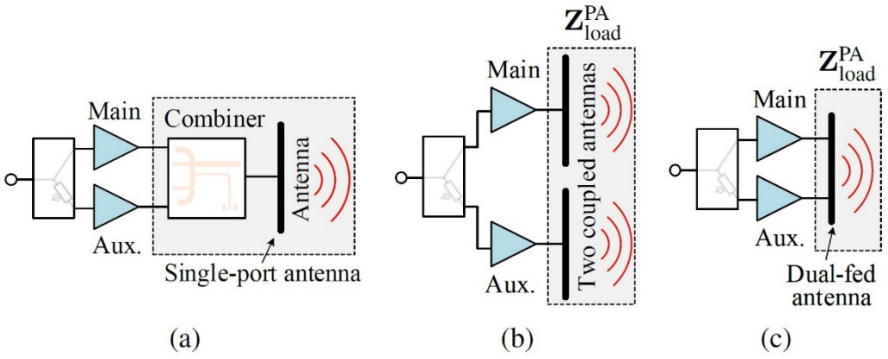


Figure 5.3 The evolution of DPA-antenna integration concepts (from [40]). From a lossy separate power combination (a), to the use of antenna elements for load modulation (b) and to electrically small DPA-antennas module (c).

# 4 System architecture definition and development of RF synchronization concepts

In order to make the concept of massive MIMO truly Distributive in nature, it is essential to allow large groups of neighboring nodes to form virtual antenna arrays for both transmission and reception. But to bring this concept from theory to practice requires the concept of synchronization to be applied at multiple levels in a distributive network.

Broadly this concept is classified into two main categories. One to have phase coherency between multiple transceivers on a single node to achieve maximum benefit of transmit diversity and beamforming in phase arrays, i.e. signals feeding into the transceiver units of each of the tiles should be both frequency and phase coherent. While the second category deals with achieving frequency and time synchronization between the front ends that are distributed in a cell. [41],[42].

Ideally, a user being serviced simultaneously by multiple fronts will then always have line of sight conditions with at least one of them, while the network would be adaptive enough to respond to the user. There are multiple benefits cited in favor of this topology e.g. low latency, high throughput, diversity of applications that can be serviced.

From an implementation point of view, two fundamental challenges can be identified:

- To make transceiver units frequency and phase coherent despite random phase noise and parasitic that become more critical at mm-wave operation.
- Efficient calibration algorithms to synchronize distributive nodes in frequency, time and phase without constraining data throughput of network.

### Synchronization in distributive Massive MIMO

The concept of distributed beamforming works on the basic principle of having all nodes agree on same message, transmitting at same time and carrier frequency and to also control their phases for constructive combination at the user terminal. Each node has an independent local oscillator and therefore frequency variations must be corrected against signals drifting out of alignment

during transmission. Frequency synchronization uses a Master-Slave approach in which either the user terminal or one node broadcasts a carrier frequency allowing others to synchronize to it via operations performed in DSP. Phase synchronization is essential as each node has an ambiguous phase offset which becomes a part of channel estimation process and degrades channel phase information since it cannot be disambiguated from relative phase offsets. Timing synchronization deals with same symbol transmission at same time which if not maintained can cause inter-symbol interference. However, compared to carrier phase synchronization, timing synchronization is not a fundamental bottleneck, and there are multiple algorithms that can tackle timing synchronization for low and high data rates. [41],[43],[44].

### Synchronization between separated nodes

Carrier phase synchronization is classified into two types. Close loop synchronization in which user terminal controls phase alignment between nodes by exchanging beacon signals with all nodes and then giving digital feedback to each node to compensate the phase offset. In open loop synchronization, nodes exchange beacon signals among themselves and use this beacon as well as signals exchanged between other nodes to achieve appropriate phase compensation without involving other user terminals. [41],[43].

One drawback of all these approaches is that they have mainly focused on sensor networks, and therefore suffer from the limitation of multi-user approach which is essential to scale these algorithms to cellular networks.

Recently work published in [44] has tried to solve this limitation by designing and validating algorithms particularly suited for cellular communication networks. The work considers the fact that in cellular networks distributive nodes have a central processing unit that is responsible both for exchanging data to/from user terminals via distributive nodes and for estimating channel matrix for each user. Thus, in such a scenario there is minimal requirement at user terminal to participate in the synchronization process and CPU usually assumes the position of master in a traditional master slave architecture to synchronize nodes to common frequency. The distributed cellular networks also suffer from limitations of non-reciprocal TDD channels. Ethernet connected digital backbone between CPU and nodes can provide standard timing synchronization protocols such as IEEE 1588, but cannot support a high-speed common clock.

The work in [44] shows how each node estimates channel to each user through exchange of pilot signals and send these estimates to CPU, where CPU then calculate a distributed precoding matrix. Each node then processes these OFDM encoded symbols, using a calibration block that compensates for non-reciprocal amplitude and phase rotations. A subset of nodes called anchors exchange pilots among themselves during special synchronization slots inserted in frames periodically. The noisy timing and frequency estimates extracted at each node are sent to CPU for processing by weighted least square minimization method and finally correction factors are sent back to respective nodes. Remaining nodes then get synchronized to anchor nodes. Similarly, all nodes exchange calibration pilots among them from which noisy complex amplitude estimates of receive pilots are then processed by CPU by finding calibration coefficients, solving constrained least square problem. These estimates are sent back to respective nodes which then extract

timing and frequency information from pilot signals using some suitable estimator for updating their CAL block for further use.

The solution discussed is scalable and compatible with existing architecture of user terminals. However, the author has not discussed the limiting problem of phase synchronization between the nodes, and whether the discussed methods can resolve this issue.

On the other hand, latest demonstration of distributive MIMO from implementation point of view in [45] proposes a test best solution that employs all digital sigma delta on fiber architecture. This involves the generation as well as distribution of RF communication channels from a central station using high speed optical digital components for interconnections and using conventional FPGA. The method uses sigma delta modulation to modulate an information carrying signal to 1-bit digital signal by oversampling and noise shaping which then drives a laser. The optical output is converted to electrical by a photoreceiver at other end of optical fiber from which original signal is extracted via filtering and amplification. The entire up conversion takes place at CPU in digital domain, eliminating the local oscillators all-together from the nodes' hardware, enabling highly phase synchronized signals from CPU to each node. Excellent RF phase coherence is achieved among separated nodes without any addition of signal processing on hardware.

This is flexible, low cost test and easy implementation as well as scalable architecture. But it only solves the problem for achieving coherence between two geographically separated nodes. The fact that each node hosts a set of multiple transceiver units (and therefore the use of local oscillator and mixer etc. would be inevitable in the scenario of actual massive MIMO implementation at one node) would then demand some other approach to be adopted.

In short, it would be interesting to investigate and come up with a solution for carrier synchronization that considers the multi-user environment of cellular networks as well as the Massive MIMO implementation in a distributive manner as no one solution discussed above satisfies all these requirements.

### Synchronization within one node

Achieving synchronization in terms of frequency and phase between several of the tiles (where each of the tiles host a number of on-chip transceivers and local oscillator architecture usually implemented as phase locked loop) on a single base station poses a critical performance bottleneck; if left unattended it can prove to have disastrous affects for phased array performance of network. [42], [46], [47]. To make several channels of transceivers phase coherent from a single base station therefore is of paramount importance. The approach usually adopted is to make use of some calibration mechanism that tends to remove phase offsets between the transceivers of each channel periodically in order to make them more coherent. These phase offsets exist within the transmitter, receiver architecture as well as within local oscillator architecture.

However, the synchronization process for local oscillators is complicated by the fact that it involves two fundamental problems of phase noise and LO drift as function of temperature & time. Both issues are random with respect to time and cannot be calibrated out. In such an instance two obvious choices would be to either

- Reduce phase noise and LO drift to such an extent that channel-to-channel variation does not remain a bottleneck.

OR

- To design a LO sharing architecture such that channels become coherent despite the variations

One of the most popular techniques currently being employed in state of the art of Massive MIMO systems is the H-tree technique. In this method, a single Reference Clock is routed across to each of the phase locked loops in each tile making use of power divider ensuring synchronized behavior. One of the latest works that has incorporated this technique for achieving synchronization in a phased array is [47]. In recent years all digital PLLs have been extensively used owing to precise full digital control of loop functionality. In this work phase array performance is demonstrated at 60 GHz using digital beam steering capability for MIMO transmitter by making multiple ADPLLs phase coherent using calibration method. The protocol for phase alignment is tor carry out a cancellation method in order to acquire out of phase state between two ADPLLs.

Although having easy design, this method suffers from some critical limitations; namely scalability issue i.e. design becomes extremely complex with high number, power constraint on reference clock to drive loads with same high power as number increases, requiring external hardware + software calibration mechanism to calibrate out the phase offsets e.g. by using adaptive phase shifters and most importantly inability to calibrate out channel-to-channel variations due to each PLL being independent.

Another technique that has been used lately is termed as Daisy chain technique. Its principle of operation is that each phase locked loop becomes a reference clock for each subsequent phase locked loop. Reference clock itself only feeds the first phase locked loop. Thus, each PLL compares its generated signal with the clock signal of previous PLL. Complex distribution network for reference clock is no longer needed (reduced footprint) and no constraints on the output power of reference clock. Phase offset between the PLLs becomes lower due to reduction in LO drift because of using high frequency PLL as reference for each subsequent PLL.

This technique has been intelligently adopted recently [47] by demonstrating a W-Band integrated 384 element phased array. In this work instead of using the output of each PLL directly as input, a frequency lower than output frequency (~ 90GHz) at 27 GHz clock is used between the slave nodes. This reduces incoherency between channels due to LO drift as a result of lower multiplication factor and lower amount of voltage noise being translated to time noise as a result.

Daisy chain technique has a limitation however, as the number of PLL increases, the phase noise progressively becomes poorer in performance and as a result there is more incoherency among channels.

The techniques of coupled oscillators and coupled phase locked loops have recently emerged as superior alternatives. The techniques were originally employed as alternatives to analog phase shifters by using oscillator elements directly to create the required phase offsets making use of injection locked technique.

The work [48] for example is based coupled oscillator theory to generate multiple phases, Both the simulation and experimental results of the work show that the as the Number of oscillator cores N increases, the phase noise decrease by the amount $10\log_{10}N$ , and the number of phases required can be expanded easily by adding one more resonator core. This work basically transforms the conventional dual tank resonator to be based on one transformer which allows strong mutual coupling of phases between the oscillators, and leveraging adaptive feedback combined with dual-tank topology can achieve low phase noise as well.

Similarly, in [49] it's shown how phase controlling signals are applied separately to each of the oscillators in order to detune their natural frequencies of each of the oscillators, while a common injection locked signal is provided to each of the oscillators via power distribution network. This method not only aligns the oscillators to the common frequency of injection locked signal but also allows control of constant phase progression as one move across the linear array of elements. Thus, it allows an efficient method of beam-steering the phase array without incurring additional power & area employed usually for analog phase shifters. However, the free-running or natural frequencies of each of the oscillators should be within the collective locking range, and the frequency of injection-locked signal should not be very different from the natural frequency following a relation given by Adlers equation. If these conditions are maintained, then all oscillators synchronize to a common frequency. This methodology is especially very useful for mm-wave based phased arrays where substrate space is scarce.

In the work [50] the authors have designed and implemented a hybrid wave oscillator which consists of rotary wave oscillator as heart of oscillator system which then couples its quadrature outputs to other distributed mixers/transceivers through standing wave oscillators. This array of distributed coupled oscillators proves to be an efficient solution in for mm-wave based applications utilizing less power and giving lower amount of phase noise. In mm-wave communications systems the intrinsic limitation of link budget performance is compensated by making use of phased arrays. The work shows that with proper coupling of oscillators it is possible to reduce the phase noise of each oscillator and that improvement thus leads to lower usage of available power by demonstrating a 4-element array of oscillators mutually coupled at 54 GHz frequency.

Although the injection locked oscillators seem like a convenient solution to beamforming in phased arrays or to achieve coherent output signals, they have some limitations inherent in their architecture. The phase dynamics and locking range of Injection locked oscillator depends on the quality factor of oscillator, the magnitude of the injected signal strength. Thus, they suffer from low locking range, and non-uniform amplitude of output waveform in the instance of frequency detuning, leading to more serious problems once the array size increases. Thus, coupled PLL technique offers superior results as far as locking range and amplitude performance is concerned.

This work [51] mainly focuses on the phase dynamics and phase noise performance of N coupled PLL systems with independent oscillators and verify their model by implementing the design at X-band using MESFET GaAs technology. The work summarizes that it's possible to reduce the near-carrier phase noise of single PLL in an N-element array to 1/N that of single VCO in the PLL; provided the feedback loop gain is large, the network is reciprocal, and the PLL components noise can be ignored.

In the work [52] the author has mainly focused on making use of Type-2 PLL topology in coupled PLL configuration and using an external reference signal in order to achieve beam steering performance in a phased array. The reference frequency allows the antenna array to stably stay synchronized to constant output frequency while a single control voltage steers the beam having the capacity to reduce the beam-point error that arises due to phase errors in the oscillator array. Circuit fabrication inconsistencies lead to changes in the free-running frequencies of oscillator which as a result cause phase errors and affect the beam-pointing performance. Likewise, these fluctuations can also impact the common frequency of oscillator array leading to deviation from the design frequency. These fluctuations also prove to be a bottleneck in the performance of coupled Phase locked loops if PLL is of Type-1 topology. With the type-2 PLL topology adopted in this work prove to be much more stable in terms of output frequency and the resilience of architecture against such fluctuations.

The work in [53] is the most recent and promising result as far as application of coupled PLL in the synchronization is concerned. The work improves upon the limitations of two-wire bidirectional coupling of phase locked loops by making use of single wire architecture using quadrature coupler at the input of each of the phase detectors in a single PLL IC. The architecture reduces the phase noise and is also a compact solution compared to two wire approach and can be readily employed in the tiled approach scaling of MIMO systems. Additionally, the structure make use of Type-2 PLL and includes variable phase shifters in each PLL cell to compensate for static phase offsets between the LO ICs which is undesirable for an application that doesn't make use of phase array performance into its design.

### Phase noise reduction techniques

From the hardware implementation perspective, phase noise of a frequency synthesizer poses a critical bottleneck to achievable data throughput. The communication system using OFDM modulation schemes is especially susceptible to phase noise variations as it tends to generate an effect which is quite like inter-symbol interference thus limiting the overall maximum achievable capacity by severely affecting EVM [54]. One classical way is to improve the phase noise performance of an oscillator. The design in [54] focuses on a topology such that the overall phase noise reduction in the PLL loop can meet the stringent EVM requirements in a 64 QAM communications link at 5G frequencies. The oscillator consists of single core, lowest power supply value for that technology, and makes use of cross coupled design that utilizes the transformer coupled resonant tank. The transformer coupled resonant tank takes care of practical limitations in the layout of LC circuits as well as create harmonic resonances. The design results showed that by tuning the VCO harmonic impedances it's possible to reduce flicker noise, phase noise as well as to reduce DC power usage. The final design is incorporated in a charge pump-based type-2 PLL architecture that precedes multiplier circuit having the ability to generate LO frequencies in the frequency range of either 28GHz or 39GHz band.

The tradeoff between phase noise performance and power consumption become critical at mm-waves. At these frequencies not only, low-quality factor yields high out of band noise but implementing a chain of high frequency divider further degrades the power performance. To

achieve low in-band phase noise a high division ratio is required in the PLL feedback path that demands high power consumption posing a bottleneck to low power low noise PLL design. In the work [55], the author has made use of low power 20GHz sub sampling PLL which allows much lower in-band phase noise, preceding a 60 GHz injection locked QVCO which helps to boost to negative transconductance & reduce power consumption. In addition, a dual step-mixing injection locked frequency divider saves battery power, improves locking range and enhances gain of QVCO by tail coupling technique resulting in low noise low power PLL at 60 GHz frequency achieving a FOM of -236.

Continuous scaling of CMOS technologies in the years has led to poor analog performance while frequency synthesizer has traditionally been an analog component. This has led the engineers to seek all digital solution to PLL design, even though VCO and TDC components in PLL loop are still analog in nature, dictating fundamental limits on the phase noise. The subsampling technique through the removal of frequency divider and charge pump has allowed in achieving excellent figures of merit and total integrated phase noise performance but has enjoyed less popularity due to its Integer N operation and serving as bottleneck to the congested frequency spectrum in wireless communications. This work [56] makes use of subsampling fractional synthesizer by employing digital to time converter instead of time to digital converter that overall not only makes the system much simpler but also allows fractional N performance, and achieving a large tuning range from 9.2-12.7 GHz, and very good integrated phase noise performance of lower than -104 dBc/Hz. In this work modulating the phase of the reference which is conceptually equivalent to the behavior of modulating the frequency divider in classical PLL design is used. This DTC is inserted in the path of the reference clock and is used along with Integer-N PLL allowing quantization error to be known as a priori. Modulation is also adjustable to counter PVT variations by making use of online calibration

The conventional or classical PLL architecture performs very poorly at mm-waves due to poor phase noise resulting from large division ratio, inferior CMOS transistor and low tank quality factor. A classical type 1 PLL has certain limitations ranging from inability to suppress VCO flicker noise, low loop gain and limited locking range, locked state with non-zero phase shift and large spurs. Although, the sub sampling technique does improve the in-band phase noise, but this method has a tradeoff between the frequency resolution and acquisition range. Moreover, taking power consumption into account, it becomes too power costly to generate wide-band quadrature signals except by using quadrature VCO. The work in [57] accomplishes both high wide acquisition and high frequency resolution by making use of cascaded PLL architecture and achieving low phase noise and power consumption by employing injection coupled quadrature VCO in the architecture. The first PLL makes use of fractional architecture of PLL providing 2.7-2.8 GHz reference to second PLL that allows wide acquisition range for second PLL and employs modified charge pump to reduce spurs. The second PLL makes use of quadrature VCO with sub sampling architecture. The cascaded PLL can achieve -177 dBc/Hz of phase noise from 93.4-to 104.8 GHz frequency range

An alternate approach solving the phase noise issue has been shown recently, through coupled oscillator theory, [58] which is traditionally used to achieve beamforming in systems. In doing so they demonstrate that phase noise reduces as the number of coupling oscillators is increased at

the expense of power consumption and area. This technique thus improves phase noise performance of oscillator via injection locked technique of coupled oscillators. Even though power is increased, the overall FOM is kept constant by increasing the magnitude of output swing voltage. In order to not have reliability issues with increasing output voltage swing and to efficiently make use of DC power consumption the inductance of resonator is reduced up to a limit beyond which it degrades the phase noise performance which is a function of technology.

In order to improve performance at mm-waves, a sub-harmonic injection locked technique can also be utilized to reduce phase noise contribution of VCO by providing clean reference, but this method suffers from low locking range, and is very sensitive to PVT variations especially at mm-wave frequencies. In order to carry out the frequency alignment between injection locked reference and VCO, very strict phase relationship must be maintained which is usually achieved by making use of delay locked loop or injection time calibration leading to more power consumption. Frequency locked loop is another method to achieve precise relationship for frequency alignment and makes use of frequency divider and frequency detector which again leads to high power consumption. The work in [59] is based on divider less subharmonic injection locked quadrature VCO for frequency alignment adaptively aligning the control voltage to QVCO. Additionally, the QVCO employs current reusing topology which consumes low power and transformer coupling in order to widen the locking range.

The work [60] also makes use of cascaded PLL design, with the first PLL offering fractional division performance while the second is quadrature PLL is divider less, making use of sub-sampling concept. The fractional division in the first stage PLL yields very low quantization noise by making use of high-resolution phase mixer. Compared to the single stage counterpart, the cascaded version achieves significant performance improvement both in terms of power consumption and phase noise at mm-waves and can achieve stringent requirements posed by the 5G Transceivers from 26-32 GHz frequency band.

The large ratio between the reference frequency and output frequency alleviates the noise limitations of the overall PLL system, but on the other hand it also leads to increased lock time. This reference frequency is several hundred times the loop bandwidth. This is done by interfacing mm-wave PLL with another PLL that provides this reference frequency. Thus, this paper [61] focuses on mode-switching architecture which switches between fast locking mode (for first 3 us) during the first part of settling period and then low noise mode that achieves record low power consumption resulting in the lowest FOM reported for 60 GHz PLL operation. An output frequency centered around 54 GHz, mm-wave based PLL is demonstrated.

Design of frequency synthesizers at mm-waves is challenging not only because of achieving low phase noise values is more difficult but also achieving fast settling times (this is essential in order not to lose data when data rates are very high during frequency locking) at mm-waves becomes more cumbersome which imposes certain limitations on their overall figure of merit. The circuit in [61] intelligently has made use of double injection divide-by-3 circuit improving the power consumption and frequency locking range. and reducing current mismatch in Charge pump leading lower phase noise

Si-Ge BICMOS technology has shown promising results in providing high FOM at mm-wave frequency bands especially in the frequency range above 90 GHz which is the targeted frequency for this project. [54], [62]. With this technology excellent values for phase noise and flicker noise have been achieved making use of simple oscillator and PLL design topologies while the footprint area or power consumption does not pose a limitation to the system performance metrics. In the work [62], a W band PLL is designed from 92-100 GHz, in Si-Ge 0,13 um, an output power of 6 dBm, phase noise of -106.5 dBc/Hz. The design utilizes the simplicity of fundamental mode PLL while achieving high frequency and low phase noise as well. It makes use of Miller frequency divider which gives a nice compromise between low power consumption and high locking range to the PLL loop. And is overall the highest performing PLL solution at this frequency for fundamental mode PLL and is a compact solution

# 5 Architecture and technology choice for power-efficient mm-wave Front-Ends

Transceiver design is one the most fundamental challenge related to the implementation of a DM-MIMO system. Among variety of existing solutions in terms of architecture, process technology and performance characteristics, a suitable solution must be determined that best meet requirements for this application.

### Phased array architecture

There are many well-known mm-wave transceivers based on the phased array architecture. This conventional architecture has already demonstrated its suitability for Massive MIMO applications [63]. RF phase shifting array architecture is the most frequently used due to its lower power consumption.

In most recent works, one can find various additional enhancement techniques for such transceivers. For instance, the transceiver presented in [64] consists of sixteen 2x2 beamforming TRX chips. The use of such configuration results in design scalability to any necessary size and in ability to operate without preliminary calibration. Each TRX chip has NF of 4.6 dB in the Rx mode and 10.5 dBm OP1dB in the Tx mode. The IP1dB is -20 dBm per channel. The authors also underline low-cost manufacturing due to PCB design of the transceiver. Among possible enhancements is dual-polarization operation in both Tx and Rx modes, demonstrated in work [65]. Presented silicon-based transceiver consumes 143.8 mW and 103.1 mW (per element) in Tx and Rx mode, respectively. Each TRX element demonstrates OP1dB of 13.5 dBm, saturated output power of 16 dBm and has 6 dB NF.

In [66], the authors managed to reduce the transceiver area twice in comparison with conventional one by using bidirectional architecture, which is another improvement especially valuable for possible implementation in Massive MIMO. The measured NF is 5.4 dB, output power is -4.2 dBm. The transceiver consumes 94 mW in Tx mode and 105 mW in Rx mode.

Efforts to reduce the power consumption have been made in [67], which presents TRX frontend for mobile user equipment phased array. It is based on bulk CMOS due to some advantages this technology possesses, e.g. low-cost manufacturing. Designed transceiver consumes 137 mW/channel in Tx mode and 37 mW/channel in Rx mode. It has output P1dB of 14.6 dBm and corresponding PAE of 21.9%. Measured NF and IIP3 are 5.5 – 6 dB and -8.5 – -6 dBm, respectively.

### Mixer-first architecture

Relatively new architecture solution for mm-waves is called mixer-first. It aims to achieve low power consumption without sacrificing the linearity through eliminating LNA from the input stage. This approach has been already successfully implemented for sub-6-GHz systems. However, its application for mm-waves demonstrates many challenges, e.g. minimum achievable NF worsening.

The mixer-first design, presented in [68], applies additional techniques for wideband matching, such as the reduce of mixer switches size and the use of shunt resonator before the matching network. The most significant feature in this design is power consumption of only 12 mW, which is significantly lower then achieved in previous designs. The NF is 8 – 12 dB, IP1dB is -16.8 – -24 dBm. In general, the characteristics of this design let assume its applicability for massive MIMO.

### Technological process

Considering the absence of specification in terms of technology required for DM MIMO, let us look into some of the most successful LNA and PA designs based on different technological process, as an example.

The work [69] presents power-efficient LNA, based on 22-nm CMOS FinFET technology. It has 2-stage stacked-cascaded differential design. It has NF of 4 dB, the peak gain of 20 dB and IP1dB of -22.8 dBm. This LNA demonstrates high performance in terms of gain and noise figure, maintaining quite low power consumption of 10.8 mW.

In [70], both E- and W-band LNA are presented. They are based on GF 22-nm CMOS FD-SOI process and have 3-stage cascode architecture. An important feature of this paper is that these LNAs have been designed to achieve different properties. Thus, the E-band LNA was supposed to have as low power as possible, when W-band had to have much wider bandwidth. The power consumption of these designs equals 9 mW and 16 mW, respectively. Besides, their bandwidth is 12 GHz and 31 GHz. The 9-mW LNA has minimum NF of 4.6 dB and the gain of 20 dB. The 16-mW LNA, in turn, has the NF and the gain of 5.8 dB and 18.2 dB, respectively. Their IP1dB equals -27.4 dBm and -22.8 dBm.

As an example of LNA based on 0.13-μm SiGe BiCMOS technology, the work [71] can be considered. It is 4-stage cascode amplifier, consuming 28 mW, which can be assumed also not too high, considering its performance. The minimum NF is 4.8 dB, however, the IP1dB is -37.6 dBm. Higher gain (32 dB) and much wider bandwidth (52 GHz) make this a good example of LNA implemented in this technology.

Similar to LNA, PA can be implemented in various technologies. Power amplifier presented in [72] is based on 250-nm InP HBT. This W-band PA demonstrates 20 dB gain, output power of 20.8 dBm and maximum PAE of 24.7%.

The next example [73] is four-stage PA based on 65-nm CMOS. It achieves higher gain – 28 dB, output power is 16.3 dBm, but PAE equals 14.1%, which is less than in previous case. However, the PA area is reduced and equals 0.714 $mm^2$ instead of 1.15 $mm^2$ of previously mentioned PA.

In [74], PA operates at much higher frequencies – 168-195 GHz. It has been made using 130-nm SiGe BiCMOS process. The PA uses 3-stage cascode topology and achieves a gain of 23.6 dB and maximum output power of 18.7 dBm. The maximum PAE is 4.4%.

Thus, we can conclude that various technologies can be used to achieve performance applicable to different MIMO systems. The main issue is to find a trade-off between all the characteristics to ensure power efficiency and high performance at the same time.

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