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MyWave

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Report on Best Practice Cookbook

Deliverable D2.4

V1.0

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ERICSSON NXP United Monolithic Semiconductors ANTENNA COMPANY APWAVES

Document history – List of changes

Version	Date	Author name	Scope
V1.0	30/01/2023	Rüdiger Quay	Report on Best practice cookbook.

Contents


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1 Introduction

This document describes the design flows reviewed and updated by the ESRs after 28 months into the project MyWave. 14 PhDs are working on their theses, and the following report gives an short overview on their status with respect to the proposed design flows and best practices established in the education and research work for mm-wave antenna design and deployment for next generation communication. With the beginning of mm-weave usage in real radios in 5G, these techniques will be beneficial for European system deployment up to the years 2030.

2 Updated results at the end of the project

This document describes the latest findings by the ESRs after 28 months into the project MyWave. 14 ESR are on a good path to submit technical papers on the level of the state of the art, which are by now starting to be submitted and accepted.

Some generalized findings per topic of the ESRs are summarized in the following to give an overview of the overall activities.

2.1 ESR2: Best practices design guidelines to cope with uncertainty propagation through the design cycle

The *all-in-one* finite element method (FEM) was the chosen flow for EM simulation design in this project. As described in deliverables 2.2 and 2.3, due to the high complexity of mm-Wave electronics designs, this approach can cause the simulation to use prohibitively large amount of computational resources. One of the ways to tackle this problem is to discretize (mesh) the simulation domain with the design heuristics in mind. Reducing the total number of discretization unit cels (tetrahedrons) by reducing the mesh density where the EM phenomena

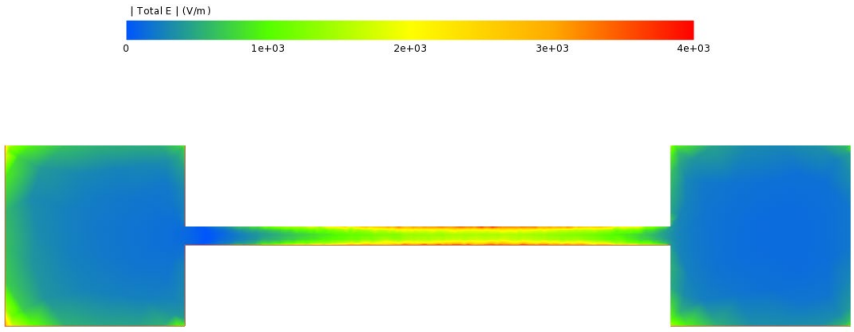


Figure 1: E-field distribution in the direct vicinity of a simple microstrip at 20GHz.

don't substantially change. Commonly, the areas with the most changing EM phenomena are in the direct vicinity of the signal traces. Figure 1 shows a colorcoded E field distribution for a simple microstrip trace excited with a 20GHz signal. It is visible that the field distribution is changing with the width of the trace, thus, the mesh of this design should be constructed accordingly.

Figure 3 shows the comparison of the old mesh and the mesh generated by the Acutomatic Conductor Meshing (ACM) algorithm designed in this project. This algorithm allows for mesh generation adapted to the trace widths through the whole design. Table 1 compares the number of tetraherons (as a measure of memory requirement) with and without ACM required for the final solution of the example on Figure 1. In this simple case, ACM reduces the simulation memory and time requirement by 55% and 17% respectively. Scaled up to larger and more complex designs, this resource requirement reduction becomes a signiticant improvement of the EM simulator's capabilities making it the best practice in *all-in-one* EM simulation flow.

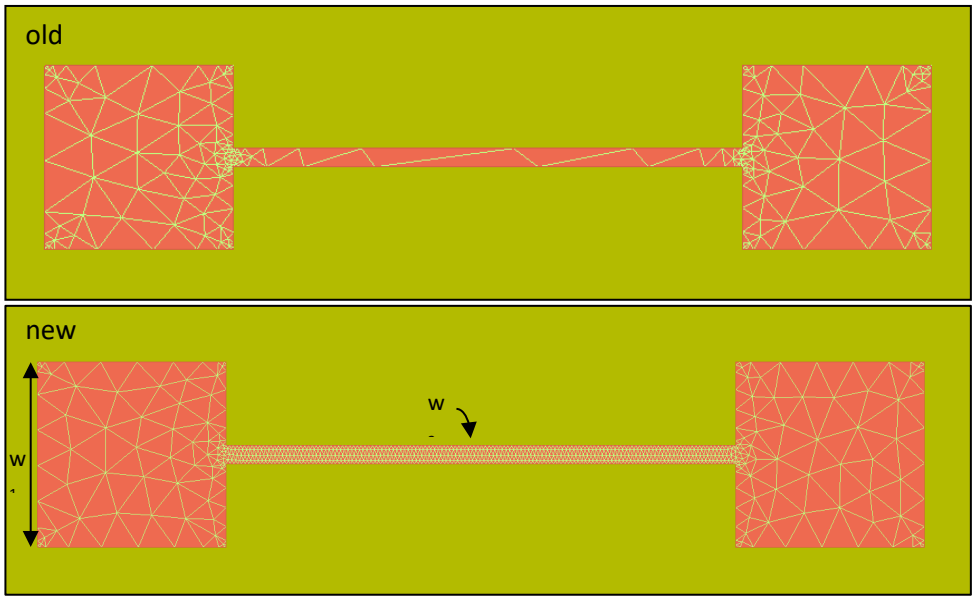


Figure 3: Comparison of the two meshes, with and without the ACM algorithm

Table 1: Comparison of the final memory and time requirement with and without ACM for the example in Figure 1

	Initial tets	Final tets	Refin-ement steps	Mesh refinement time	Total sim. time
Without ACM	2917	11063	8	6s	49s
With ACM	4749	4749	1	1s	18s

2.2 ESR3: Best practice for radio frequency integrated circuits co-design

Most of the design flows presented so far involve only a component level integration, which consist of a list of requirements to be fulfilled in a general aspect. For low frequency design that might be enough as a proof-of-concept or even for mid-scale production. When it comes to millimeter-wave (mm-wave) design is known that the challenges are not only on the circuit design level, but the whole process, namely modelling of components, manufacturing capability, proper testing protocols, etc. This forces engineers to be aware of the whole manufacturing process and actively feedback to other teams.

Designs as proof-of-concepts are missing some requirements that are set in the products, such as temperature of operation, life expectancy, and packaging. This last concept has a rapid development in recent year towards mm-wave components, as a suboptimal design may limit their performance. For several years, Process-Design-Kits (PDKs) has been major tools for integrated circuit (IC) designers to

properly implement circuits and fulfill system specifications. Therefore, package and Assembly-Design-Kits (ADKs) may become a PDK-like solution to aid package designers to meet those product requirements [1].

The design flow of radio frequency ICs (RFICs) for mm-wave applications is not different for those in low frequency, but there are guidelines to follow and ensure a proper design or implementation. In Figure 4, the design flow for RFICs in mm-waves is presented.

For mm-wave, the core sizing and interconnections are crucial as large transistors may offer larger output power, but at the cost of parasitics that may reduce the performance towards the W-band. Schematic designs may offer a quick operation insight but losses in interconnections due to low Q-factor requires a proper electro-magnetic (EM) simulation to detect possible oscillations, at this point, small signal stability checks may suffice.

When the bias strategy is selected and all interconnections are in place, the cell can be tested in small and large regime, but also doing stability check in frequency and power (!) for the expected temperature of operation, sweep of temperature is also recommended, as the DC operation point shifts with it.

Once this part is completed and the circuits operates as expected the conditioning of the circuit towards tape-out is the next step. This part consists of loops of Design-Rule-Check (DRC) and Layout-Versus-Schematic (LVS) checks to know that addition of components such as de-embedding structures and supply lines are also correct. This may take several loops to overcome.

For the testing section, measurements of power sweep and modulated signals are most common tests, also two-tone tests are usually carried out to characterize a power amplifier. The results must be compared, and if they agree with the simulations, this can be considered a successful implementation, but if there is no agreement, a troubleshooting process starts, to find the source of error and possibly find a solution.

This is a design-flow that may suffice for a proof-of-concept, but for product implementation, the packaging and other rules must be considered. In Figure 5, the ADK design flow can be observed, this considers rules that may maximize performance across components on the wafer.

As the ADK is a relatively new concept, no detailed information is presented, but rather a possible solution towards IC designers. After some trials, product optimization from ADKs may set new design rules o constraints that can be considered in the IC design flow, with this new information, this design flow could be updated and improved for the mm-wave applications.

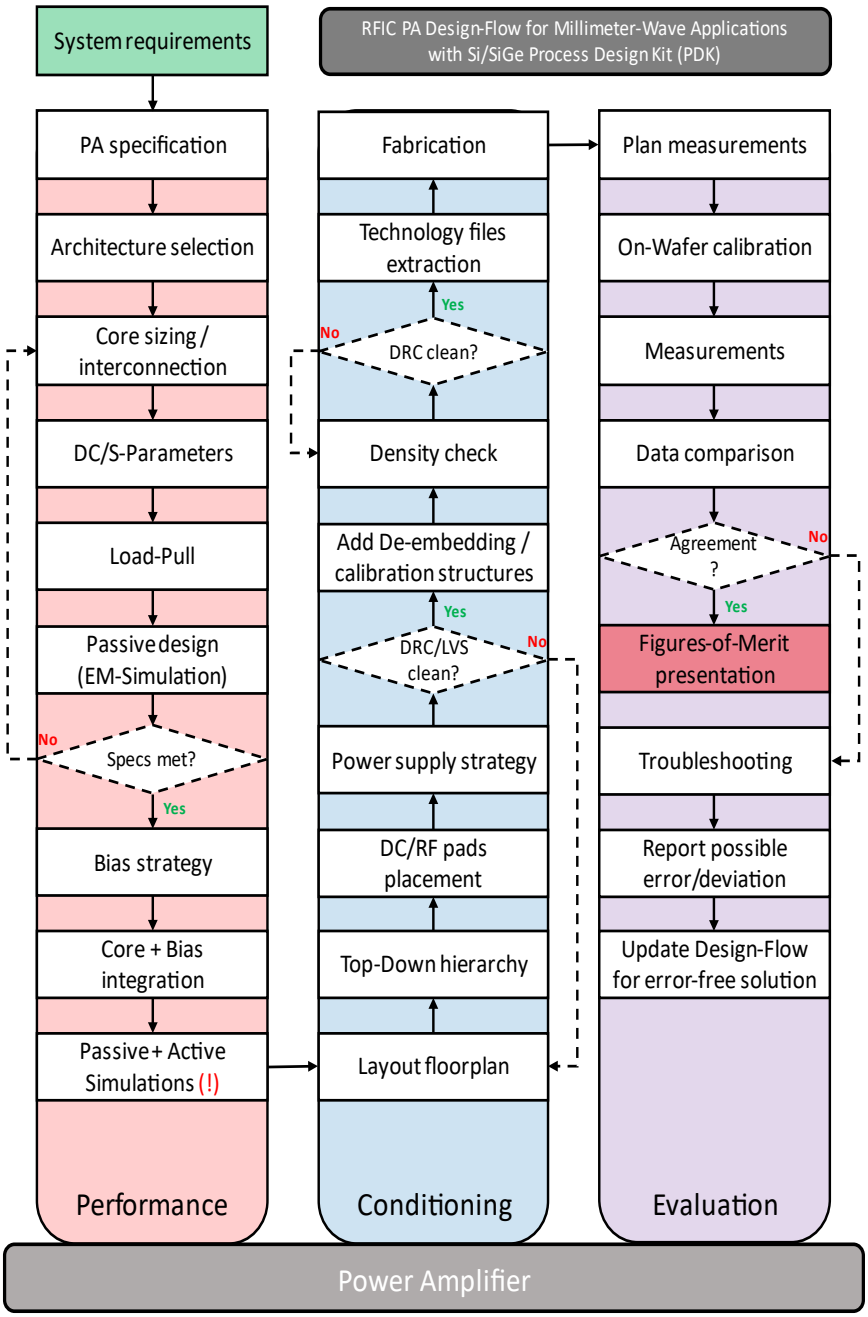


Figure 4: Design flow for RFICs in mm-wave

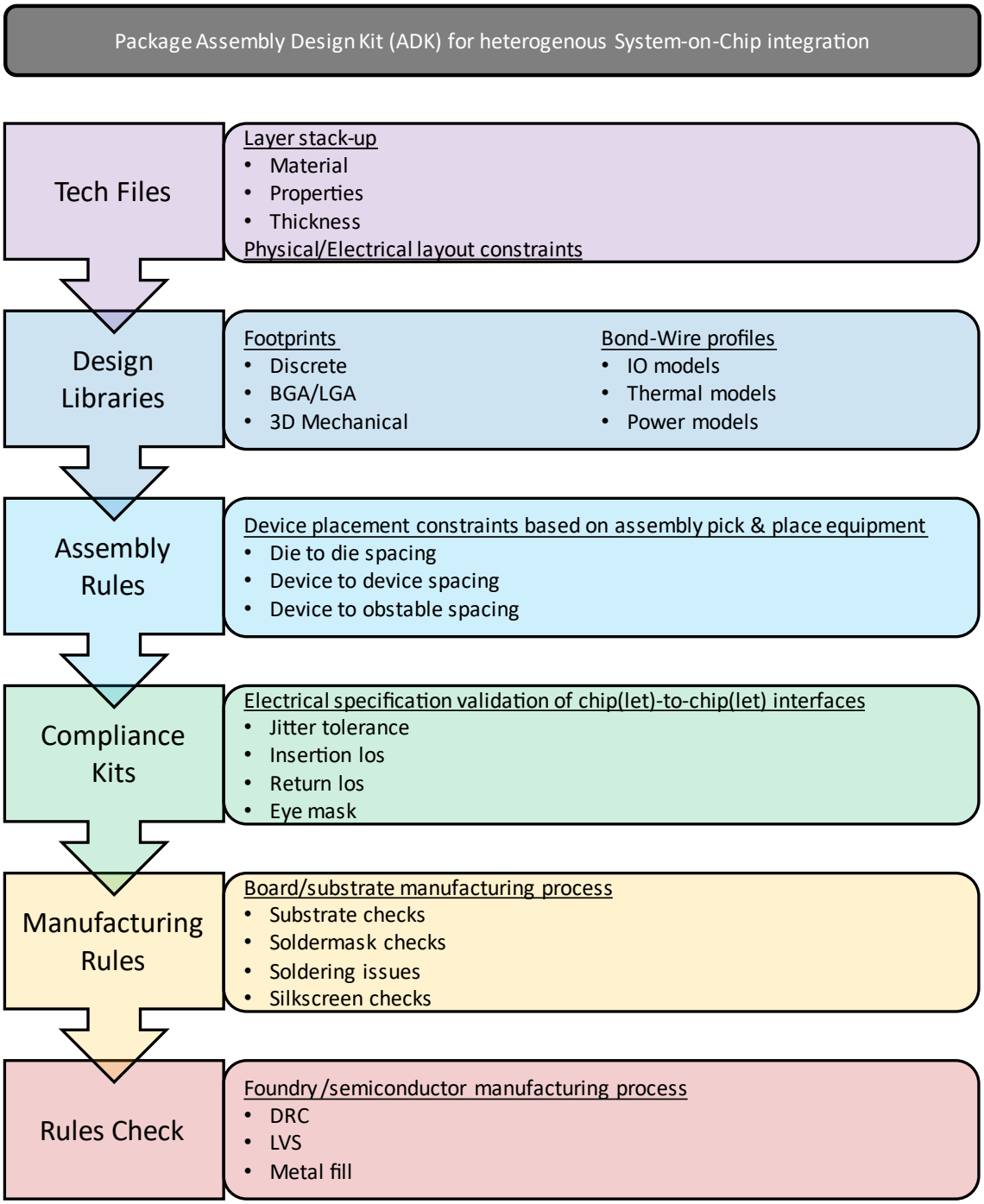


Figure 5: ADK components for IC co-design

2.3 ESR4: 100+ GHz reconfigurable wide-band wide-scan Gap Waveguide array

The future wireless communication beyond 5G holds the promise to reach Tbps level throughput at distances $\geqslant$ 1 km with flexible user mobility. The upper millimeter-wave bands (100+ GHz), especially W- and D-band, are being widely considered for these applications. This work presents a novel high-efficient and wide-beam array antenna type, which is of a particular interest at 100+ GHz owing to a contactless design alleviating active beam-steering electronics integration. A sub-array concept combining a low-order (1-bit or 2-bit) phase resolution and a spatial quasi-optical (QO) beamforming network is proposed and demonstrated in Gap Waveguide.

The present design flow is considered to start from partial components designs (antenna elements, sub-arrays, feeding networks, isolated phase shifters) to integrated combinations (sub-array with feeding networks, sub-array with integrated active phase shifters). While in practice, the major challenge in design flows is the successful demonstration of the manufactured prototypes, which almost reach the physical complexities limit of the chosen manufacture technologies (CNC-milling, PCB process, MMIC Process) in balance of reasonable cost and desired performances.

Therefore, in the updated final design flow:

The break-down tasks of a), b) & c) should be conducted in parallel.

Milestones of measurements and post-processing analysis must be reached in sequence.

These steps ensure that the prototype demonstrations in manufacturing and measurements are evaluated in time to improve and update design specifications.

a) Design the high-efficient, wide-beam array antenna that allows electronic integration.

- Design antenna unit cell & sub-array with qualified efficiency, bandwidth, and beamforming performances for beyond 5G applications. Gap Waveguide technology is chosen to ensure the high radiation efficiency and spare enough space within the waveguide that allows electronic integration for future steps.
- Design the passive spatial feeding structure for the array. A quasi-optical (QO) radial feed is designed based on numerical mode analysis in Gap Waveguide technology, which is low-loss and allows electronic integration.

❖ **Milestone 1:** The passive structures of array prototypes and array + QO feeds must be manufactured and measured to test the first-stage performances and manufacturing process tolerances.

❖ **Milestone 2**: Based on the measured results of the passive structures and active circuits simulations, post-processing analysis can predict the combined active array performances considering all system loss.

b) Codesign on-chip phase shifters (PS) to be integrated in the antenna element

- Design phase shifters (PS) circuits with low-order (1-bit or 2-bit) phase resolution in Monolithic microwave integrated circuit (MMIC) technology available at 100+ GHz. The layout of the circuits should be considered to integrate within the antenna element.
- Integrate active PS within antenna element via the MMIC-to-gap waveguide contactless transition. As no wire bonding is needed, the active antenna package is low-loss and miniaturized.

❖ **Milestone 1**: the MMIC circuits and the MMIC PS in waveguide package need to be manufactured and measured in rounds to tune manufacturer tolerances & errors until the PS circuits reach low-loss and stable phase shift conditions.

❖ **Milestone 2**: Based on the measured results of the passive structures and active circuits, post-processing analysis can predict the combined active array performances considering all system loss.

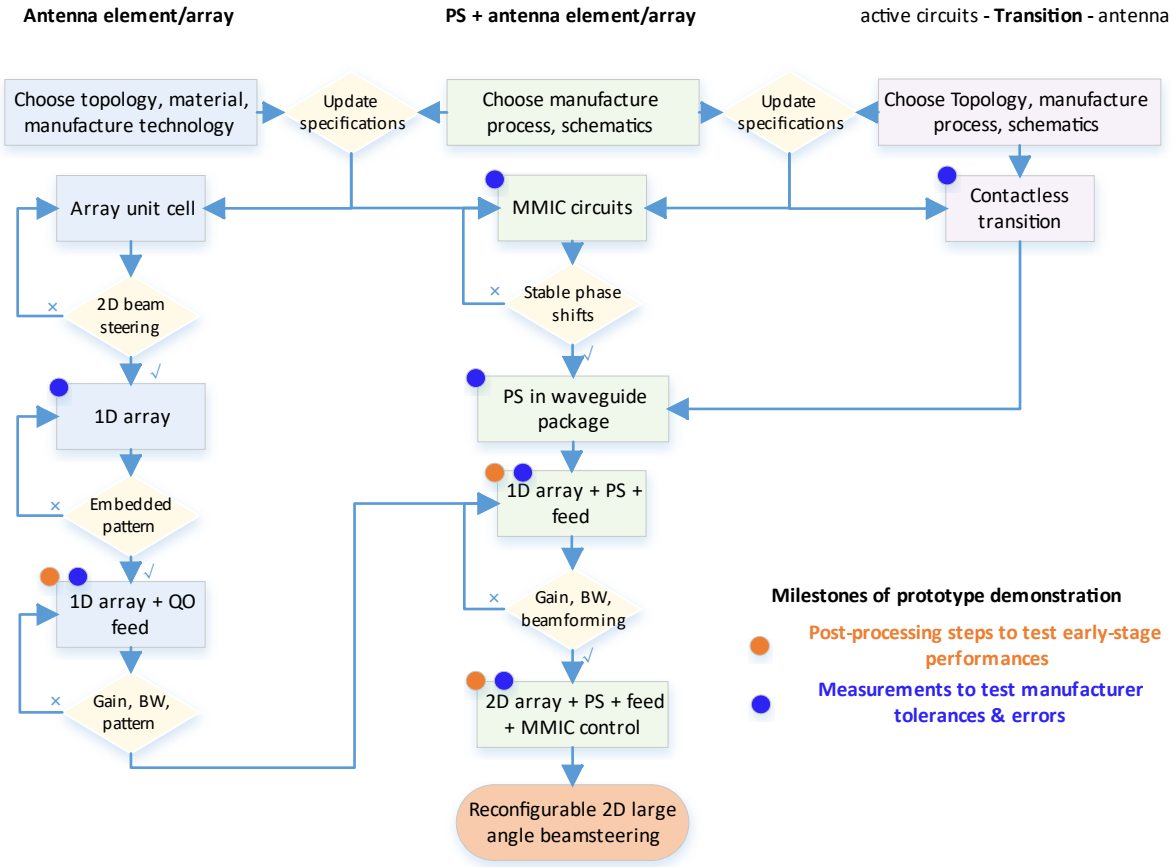
c) Codesign low-loss contactless transition between MMIC circuits and antenna element.

- Design the contactless MMIC-to-gap waveguide transition between antenna element & MMIC phase shifters. As no wire bonding is needed, the active antenna package will be low-loss and miniaturized.

❖ **Milestone 1:** The passive transition performances should be manufactured and measured to test tolerances & errors.

Final demonstrations:

This project demonstrates the concepts for active-antenna array architectures for DM-MIMO systems that can enable reconfiguration functionalities to support mobility for beyond 5G applications. The proposed 2-D hybrid beamforming network is realized by active integrated phase-shifters control and beamforming channels, in which way the system is low-cost, highly-efficient and still eligible to be manufactured with existed technology.



2.4 ESR5: Strategies for energy-efficient high EIRP generation in mm-wave wireless radio links

The goal of this project is the implementation of an initial access algorithm. Most of these algorithms are only implemented at a simulation level; however, in this project, we aim to implement them in a real scenario using a testbed. Therefore, the design flow shown below is split into two consecutive stages: algorithm simulation and validation through measurements.

The first step entails the definition of system specifications enclosing the frequency range, the radio frequency bandwidth, and the system architecture, including the antenna configuration (e.g., digital, analog, or hybrid beamforming). Afterward, it is necessary to choose between outdoor or indoor scenarios. Moreover, the channel's propagation mode and dimension are defined as the channel model's input. Several channel models, such as COST 2100 [1], 3GPP Spatial Channel Model (SCM) [2], and Winner II [3], have been standardized to be implemented according to the system specifications described above.

The mathematical description of the channel model and the proposed algorithm are required to start the simulation stage. It is essential to consider that the generation of channel models has already been standardized and needs to be rigorously followed to obtain reliable results [4] regardless of the simulation tool used by the designer. The algorithm simulation generally starts by randomly dropping the users in the chosen scenario. For each user, the large- and small-scale parameters are generated, followed by the computation of the antenna gains per azimuth and elevation angles, obtaining the channel matrix. The algorithm under test is evaluated per user and per generated channel.

The performance of these algorithms is evaluated by parameters known as the probability of misdetection (P_{md}) and the number of stages. Executing many independent experiments, e.g., in the order of 10^3 or more, we keep a record of the number of times the user received SNR below a certain threshold to determine the corresponding P_{md}. The same is done to keep track of the number of stages needed to detect the user. The algorithm metrics are then compared with a benchmark algorithm. Figure 1 gives an

example of this comparison. It shows the algorithm under test in this project (tree search) and the exhaustive search algorithm (benchmark).

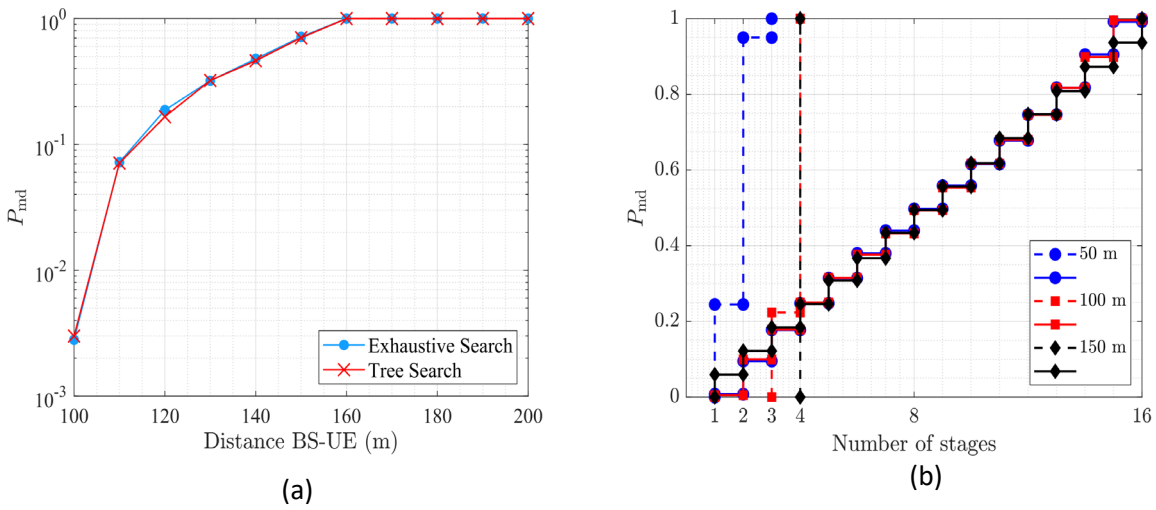
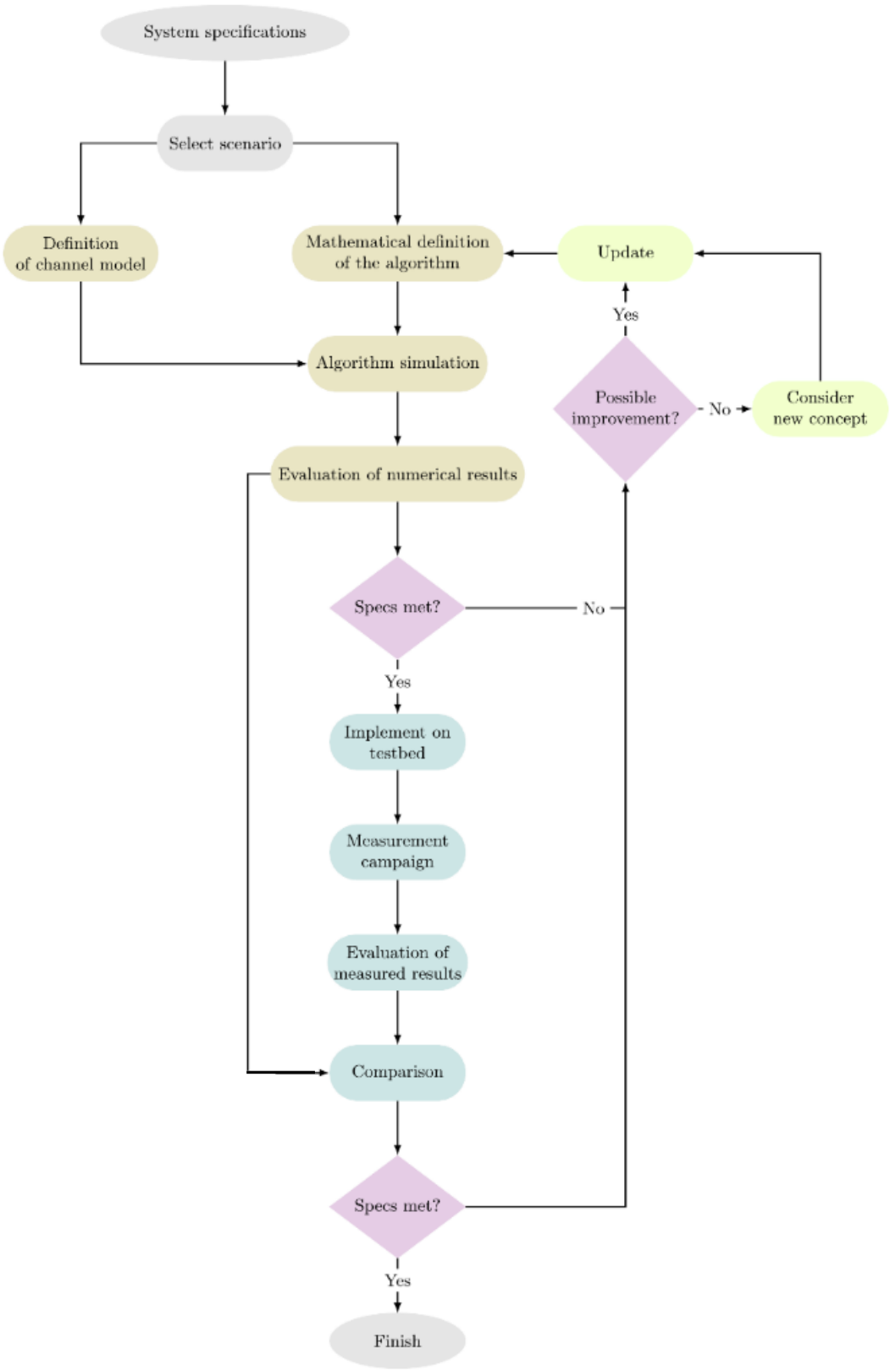


Figure 6. (a) Probability of misdetection comparison. (b) Number of stages of exhaustive search (solid) and tree search (dotted)

Once the specifications have been fulfilled at a simulation level, a measurement campaign is designed to test the algorithm in a real scenario. In this project we aim to use the testbed described in [5]. The measured results are evaluated and compared with the numerical results. If the performance specifications are met, the design has finished. This design flow can be followed to implement and test any initial access algorithm.


System specifications
Select scenario
Definition of channel model
Mathematical definition of the algorithm
Update
Yes
Algorithm simulation
Possible improvement?
No
Consider new concept
Evaluation of numerical results
Specs met?
No
Yes
Implement on testbed
Measurement campaign
Evaluation of measured results
Comparison
Specs met?
Yes
Finish

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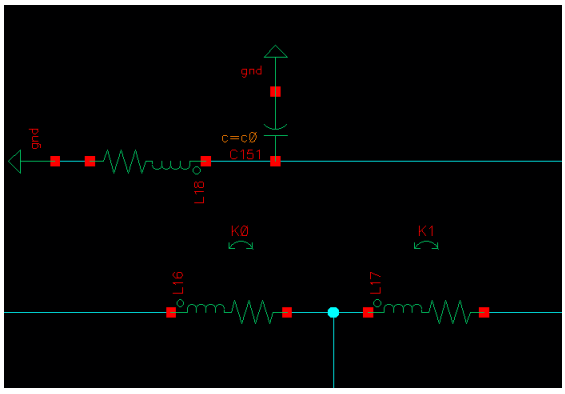
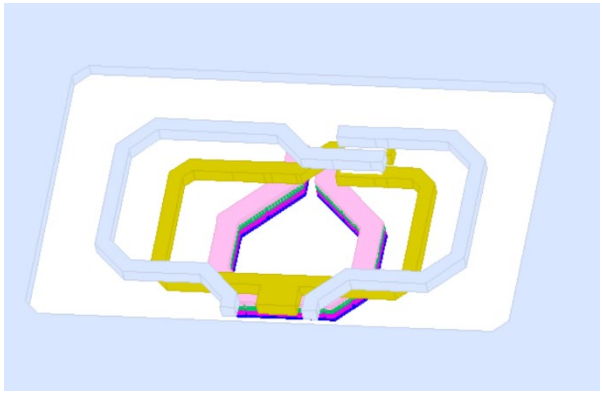
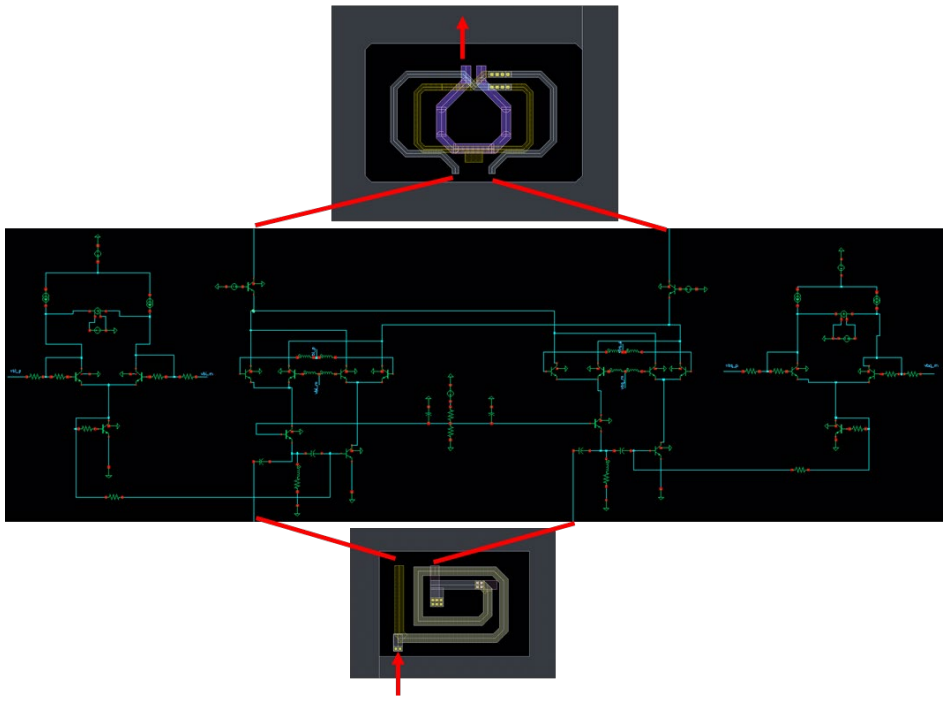
2.5 ESR6: Energy-efficient and low-cost active front-ends for DM-MIMO

Previous reports D2.2 and D2.3 present a generalized design procedure for a single electronic component and co-design of several components in a chain. This report will provide a more detailed design-flow, using a design of an active 100-GHz phase shifter as an example.

- The first step for any circuit is a schematic simulation with ideal components.
- In case of an active phase shifter, an IQ splitter mainly determines the minimum amplitude and phase errors possible to achieve. Therefore, it is recommended to create an EM model of this part and replace ideal components (90°, baluns, etc.) with EM simulated results as soon as possible.
- The use of inductors with realistic Q-factor on a schematic level additionally leads to more realistic performance of the circuit. If transformers are needed, preliminary simulation with coupled inductors can be helpful to simplify transformer design by knowing approximate inductance and coupling coefficient required by the circuit.

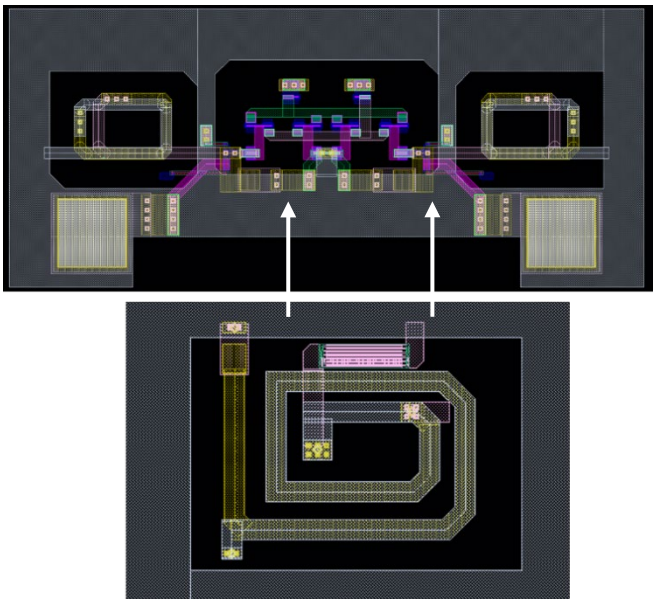






- Make an EM model of a transistor core and replace ideal connections with EM simulated ones. At this point, it is still recommended to keep a piece-wise EM simulation to have more optimization flexibility and reduce the overall simulation time. An important aspect in this case is to keep a clean interface between different layout parts. An example is shown below in the figure. The distance between input lines of the core is taken into account and output lines of the

coupler are adjusted accordingly. This approach ensures that the results after merging the layout parts will be close to piece-wise simulation results.



- After all layout parts are optimized, it is recommended to have at least one final full-layout simulation before fabrication.
- Final steps include preparation for fabrication, such as pads placement, LVS, DRC checks, fillers generation, etc.

2.6 ESR7: Analogue Radio-over-Fibre-fed antennas for massive deployment

Antenna and low-noise amplifier (LNA) co-design is a promising method for increasing the sensitivity of millimeter-wave receiver systems. Co-design involves several individual steps which usually do not intersect with each other in one design flow, but this method combines all of them together and allows to obtain mutual benefits for all components in the system.

There is no standard process for a proper co-design approach. Engineers and researchers suggested different design techniques. Table 2 summarizes information about several antenna-LNA co-design works. Due to measurement difficulties and different design approaches, it is challenging to find a common aspect among the different works. However, all of them result in an increase in performance on a system level and show the possibilities of increased gain and improved noise figures using a co-design approach.

Table 2: Overview of state-of-the-art antenna-LNA co-designs

	[1]	[2]	[3]	[4]	[5]	[6]	This work
Antenna Type	Patch	Slot patch	Triangular monopole	H-shape patch antenna	On-chip dipole	On-wafer Fshape slot	Patch
Lna Type	Common source discrete elements amplifier PHEMT	Common source discrete elements amplifier GaAs	Common source CMOS	Common source CMOS	Differential cascode SiGe BiCMOS	Cascaded CG–CS CMOS	Common source amplifier GaAs
50 Ohm LNA Gain,dB	15	16 *	18	15.3	-	23	20
LNA Gain Co-design, dB	15.5	17 *	24	15.7	27	25	19.7-20.6 *
50 Ohm LNA Noise, dB	1	1.1 *	2.5	4	-	1.9	1.9-2
LNA Gain Co-design, dB	0.65	0.8 *	1	3.2	5.2	0.76	1.5-1.9 *
Frequency, GHz	1.7-2.7	2.45–2.6	3.1-5.1	3.1-10.6	31	7	35-40

*simulation results

For this work, the founding idea of excluding any impedance transformation between LNA and antenna was proposed in deliverable 2.1. The design-flows from deliverable 2.2 are updated (Figure 7) and now it is becoming more structured and taking into account the time spent on the design process, production and measurement.

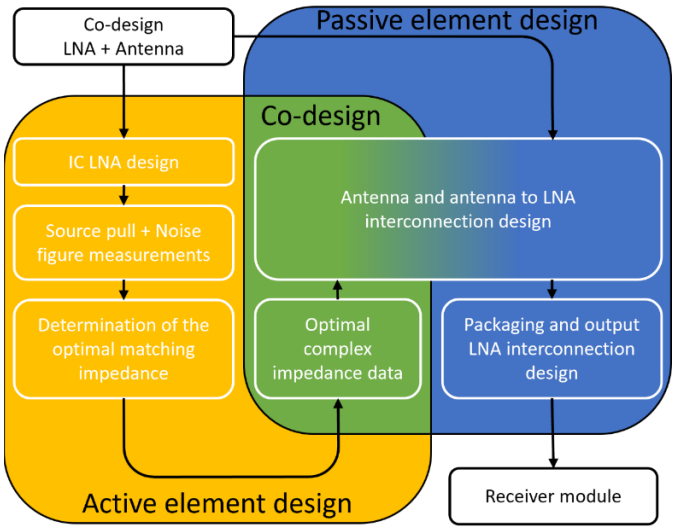


Figure 7: Main design stages

The first step is the LNA design. The chip tape-out usually took from 6 to 12 months, therefore, based on knowledge of the designed LNA model (presented in deliverable 2.3) possible to start the preliminary antenna and packaging design. After the chip production stage, the first measurement begins. The goal of the chip measurements is the full characterization of the LNA (S-parameters, noise data, optimal noise figure impedance). The result of the LNA s-parameters and source pull + noise figure measurements are presented in Figure 8.

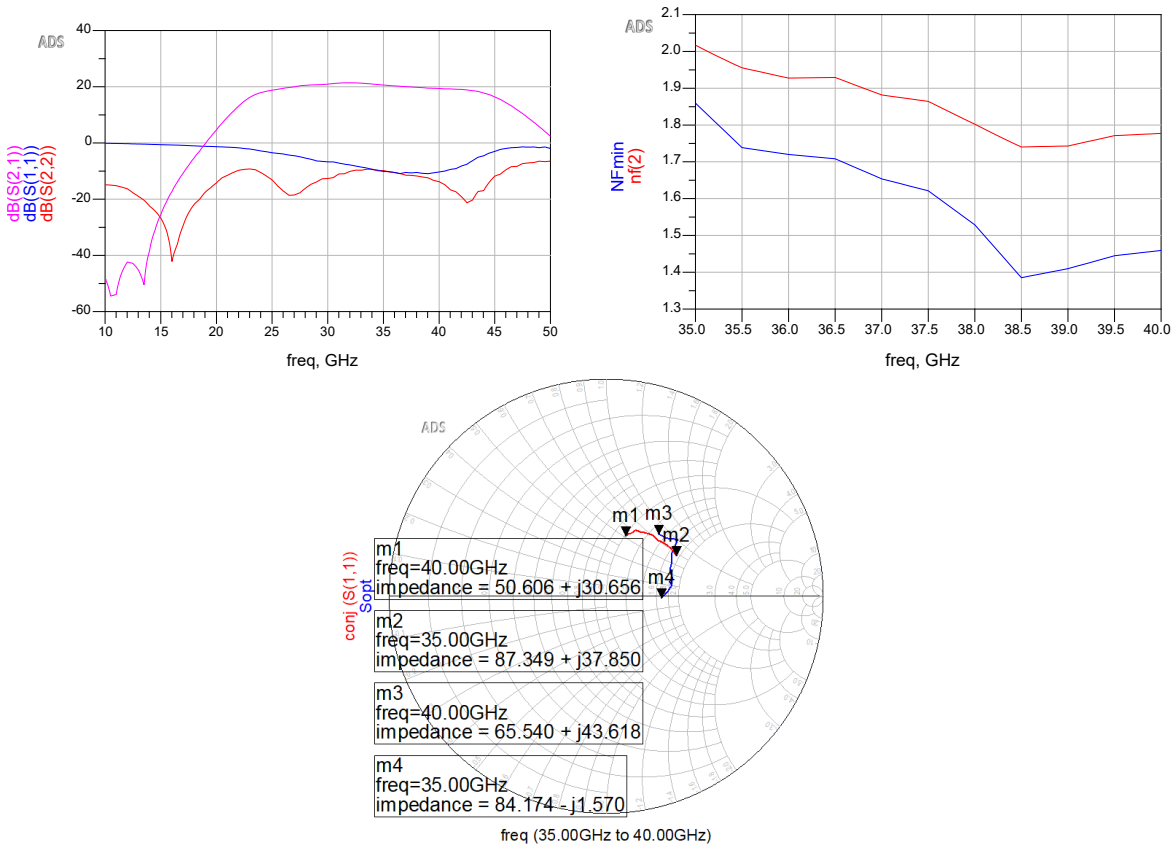


Figure 8: LNA Measurements results

The LNA noise data extraction allows getting the necessary information about the optimal impedance of the chip (Figure 8, Sopt characteristic). This data should be used for antenna optimization and interconnection design. The last step is the output 50 Ohm interconnection design to complete the receiver module for the final measurements.

References:

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2.7 ESR8: Antenna Design for 100GHz

ESR8 carried out a research project on contactless over-the-air antenna characterization, using an antenna integrated on a chip (AoC) fabricated in GaAs technology by WiN Semiconductors.

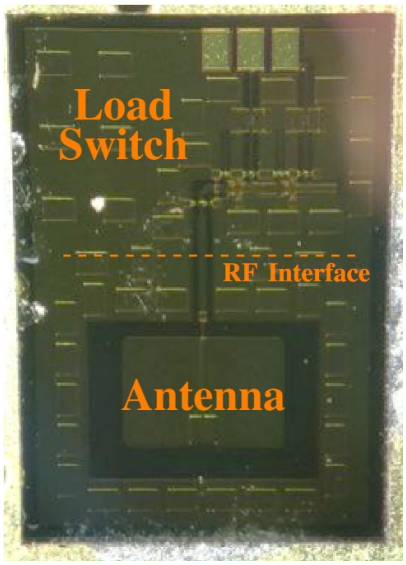

Figure 9: Photograph of the studied device. Dimensions are 1x1.2 mm^2, the antenna was designed to operate at 120GHz

Following are the most critical learnings from this project that are worth a mention in this cookbook:

2.7.1 Thermal management

In our project, we intended to vary the impedance of the antenna termination by switching the states of the load switch which in interfaced with the antenna. In the load switch design, we have used the library model for a PiN diode operating at 50mA open-state current. After fabrication, we quickly found out that when the chip is diced from the wafer and longer has a good connection to a heat sink, it presents a very small thermal mass. That lead to rapid overheating of the device in the "ON"-state. We had to reduce the "ON"-current to 10mA, but it lead into necessity to re-measure the devices on-wafer. This finding can be added to a practical advice:

- *when working with chips, take thermal management into account at the very beginning of the design phase*.

2.7.2 Effects of the environment on the AoC performance

We found that AoC is extremely sensitive to the surrounding environment. The ground plane under the device acts as a part of the antenna, and so putting anything or altering the ground anywhere within

several wavelengths from the device will affects the device's radiation pattern/efficiency. The takeaway is:

- *always model your antenna together with any objects in its vicinity*.

2.7.3 Far-field distance and the dynamic range in the anechoic chamber

The designed AoC was measured in the anechoic chamber (AC), where we were looking at the fields scattered from the device. to satisfy the far-field criteria, the device must be located at a certain minimum distance from the probe. On the other hand, the magnitude of the useful measured signal drops very rapidly as the separation between the device and the reference antenna increases. Since the surroundings of a small AoC also play a role in radiation, the effective area of the antenna might be much larger than λ^2, and the required separation then be tens and hundreds of λ. At such distances, the measured signal was so small that even the drift of the VNA of the order of -90dB starts to play a role. We recommend, that

- *when working with mmwave AoC's, be aware that the signals coming from these tiny devices are very weak. The designers should always check if the device can be measured.*

2.7.4 Antenna in package

ESR8 is working on the design of a 100GHz antenna array at their secondment at NXP.

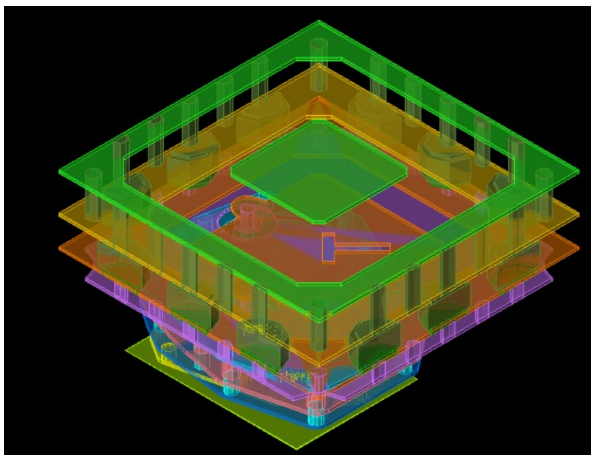

Figure 10: 3D-view of the antenna element

A couple of advices can be drawn from this project:

2.7.5 Co-design

In a complex RF system, one often can no longer neglect mutual effects and coupling between different parts of the system. Several design blocks might operate just fine on their own and fail when connected together. At the same time, in many cases it is impossible to run a full EM-simulation of the complete system due to constrains on the calculation costs. Thus, the system must be broken down into individual design blocks, but each block must be co-designed with adjacent blocks, i.e. one has to account for interaction between the blocks. A practical example of a co-design problem is antenna-PA integration, where it is not enough to just assume constant 50 Ohm termination on the PA. Antenna designed to have

a good match at 50 Ohm would have its own impedance vary quite significantly within the frequency band. This means that the PA designer should rather co-design their PA with the specific antenna. The best co-design advices are the following:

- *Adjacent blocks must have a "clean" RF interface*. What this means, is that if you want to match two circuits, both of them must be designed starting with same transmission line dimensions, with enough separation between the blocks and grounds being properly connected.
- *Not all blocks can be cascaded*. As a consequence of the previous advice, this one warns the designers that sometimes no "clean" RF interface can be created. In a practical design, the RF line leading to the antenna from the IC is composed of vias and embedded transmission line segments which are electrically small. There are also a lot of bends present in the transitions between various metal levels. If one cuts down such a design in two pieces, simulates them separately and then cascades the S-matrices, the result would differ from simulation of the whole component.
- *You have to take mechanical and thermal considerations into account in the RF design*. In wireless communications, a chip has to be integrated in a package. This package is used to route digital, DC and RF signals. It also has to provide enough heat sinking for the ICs not to overheat, and it should be mechanically robust. One has to take all of that into account, and choose the technology the materials and the stack-up accordingly.

2.8 **ESR9:** Highly efficient digital amplifier architecture based on GaN technology

The basic circuit diagram of a power amplifier (PA) is illustrated in Figure 11 where P_{DC} is the dc power supplied to the transistor through the gate and drain dc bias networks. The input matching network (IMN) transforms the impedance presented by the transistor Z_{in} to the source impedance Z_S to enable maximum power transfer from the source to the gate of the transistor. The output-matching network (OMN) transforms the fundamental frequency (f_0) optimum impedance Z_{opt} of the transistor to the load impedance Z_L. Depending on the PA topology, the OMN can also provide the harmonic impedance terminations to the drain of the transistor.

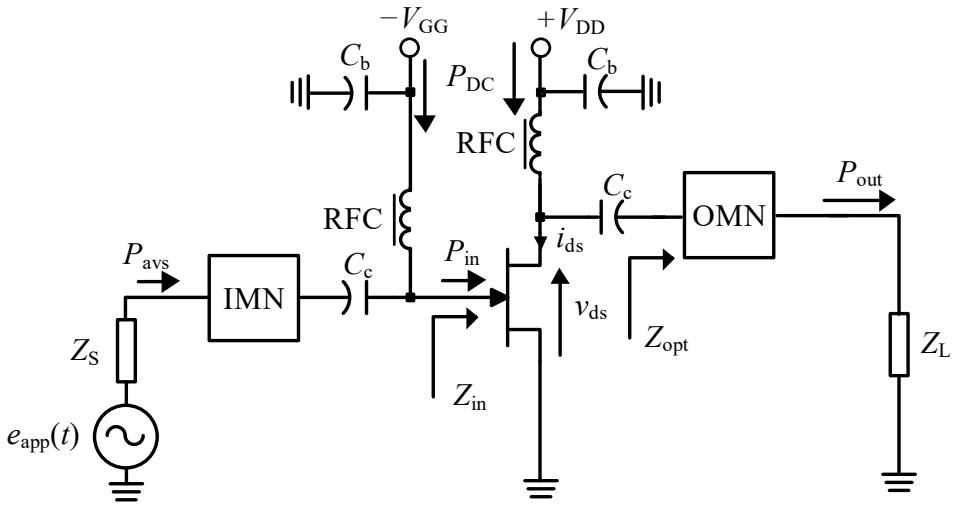

Figure 11: Basic circuit diagram of a power amplifier

The performance requirements of power amplifiers (PAs) deployed in radar and communication systems impose stringent design guidelines on PA designers. Some aspects of these design guidelines are discussed hereafter.

A power amplifier should provide a high output power (P_{out}) associated with a high power added efficiency (PAE) and a sufficient power gain over a considerably large circuit bandwidth. The first step in satisfying these requirements consists of selecting the transistor semiconductor technology with a power density capable of delivering the required P_{out}, with Gallium Nitride (GaN) being the preferred technology for high-power applications. The next step consists of sizing a single transistor for a trade-off between the maximum stable gain, P_{out}, and PAE that it can provide. A larger transistor delivers a relatively higher P_{out} but at the expense of a lower gain due to the increased parasitic elements associated with larger transistors. Consequently, the size of a single transistor is limited by the effects of the parasitic on the achievable maximum stable gain at the specified operating frequency. Thus, the need to combine several

relatively smaller transistors in parallel or series (mostly adopted in low-power density semiconductor technologies) to achieve the required P_{out}.

The power combining is performed at the transistor level, circuit level, or both. The number of combined transistors is constrained by the overall size of the circuit dictated by the desired level of system integration and the thermal requirements. At the transistor level, relatively smaller transistors are connected in parallel to form a larger device referred to as a power bar. Power amplifiers designed with such devices can deliver hundreds of Watts of power and are referred to as high-power amplifiers (HPA) hereafter. However, combining transistors in parallel results in a low load line resistance (R_{LL}) and a high equivalent parallel output capacitance (Cout) which limits the circuit bandwidth of HPAs due to the difficulty of matching lower R_{LL} and higher Cout to the standard 50 Ohm load with minimum losses.

Additionally, to extract the best performances from a power bar, it is crucial to ensure that the same impedance is presented to the gate and drain of each transistor of the power bar by the input and output matching network, respectively. Moreover, the large size of the power bar leads to a larger matching network. Subsequently, an HPA occupies a large area leading to higher production costs. To reduce production costs, hybrid design techniques are used HPAs whereby the power bar is implemented on GaN, and the rest of the circuit on lower-cost substrates. Nonetheless, this approach comes with additional constraints to take into account for a successful HPA design. The transitions between the power bar on GaN and matching networks on alternative substrates are established through wire bonding. Thus, the simulation and optimization of the matching networks, includes the effects of the wire bond.

2.9 ESR10 Efficient power combining of GaN mm-wave amplifiers

The earlier reported flow (D2.3 Milestone) is modified as per the latest experiences from the research. Due to the intrinsic characteristics of the device, the usable gain and output power at upper E-band frequencies are limited. Single transistors are unable to provide the required amount of output power. To design a higher power PA, it is, therefore, necessary to combine the power from multiple devices. Losses in the matching network have a direct impact on overall output power and power added efficiency (PAE). Therefore, additional steps are added (after characterizing the device) to design a low loss power combiner and verify using Electromagnetic (EM) simulations at the earlier stage of the power amplifier design.

The updated design procedure followed to design a PA using a low loss power combiner is given below and a generic design flowchart is shown in Figure 12.

1. This work is primarily targeted to design high power E-band (71 – 86 GHz) PA for backhaul applications.
2. At high frequencies, the intrinsic power-added efficiency (PAE) of each transistor plays a critical role in determining the maximum achievable output power [1]. Therefore, an advanced 100nm AlGaN/GaN high-electron-mobility transistor (HEMT) process [2] from the Fraunhofer Institute for Applied Solid State Physics (IAF) is chosen for this MMIC design.
3. The small-signal S-parameter simulations are performed to check the gain, stability, cut-off frequency (f_T), and the maximum oscillation frequency (f_{max}) of the selected device.
4. To determine the large signal performance, load-pull measurements have been carried out to determine the usable gain, output power, and efficiency. An optimum load target is chosen such that the transistor provides the linear output power and less gain compression.
5. With the selected R_{opt} and C_{opt} values of the transistor, a low loss power combiner is designed. This is further verified with extensive EM simulations. The combiner is optimized and verified to achieve low losses.
6. Depending on the topology selection, a distributed serial combiner or parallel power combiner is designed.
7. Stability analysis is performed to ensure the design is unconditionally stable across the frequency band. Since there are multiple stages in the design, an odd mode stability check is also performed to identify any potential instabilities between the devices.
8. With this, a Toplevel schematic is designed and large-signal simulations are performed to evaluate the overall performance of the PA. The design is further optimized to ensure that the circuit can be realizable in the layout.
9. Finally, the circuit is translated into a layout using the Computer-Aided Design (CAD) tools. Design Rule Check (DRC) is verified to ensure that the layout meets the rules set by the foundry.

10. If there are any deviations in the layout, EM simulations are checked again to ensure that the performance of the overall design doesn't deviate from the original results. The layout is optimized until the performance is met.
11. Final checks such as Electrical Rule Checks (ERC) are performed to ensure connectivity in the layout before the data is submitted to the foundry.

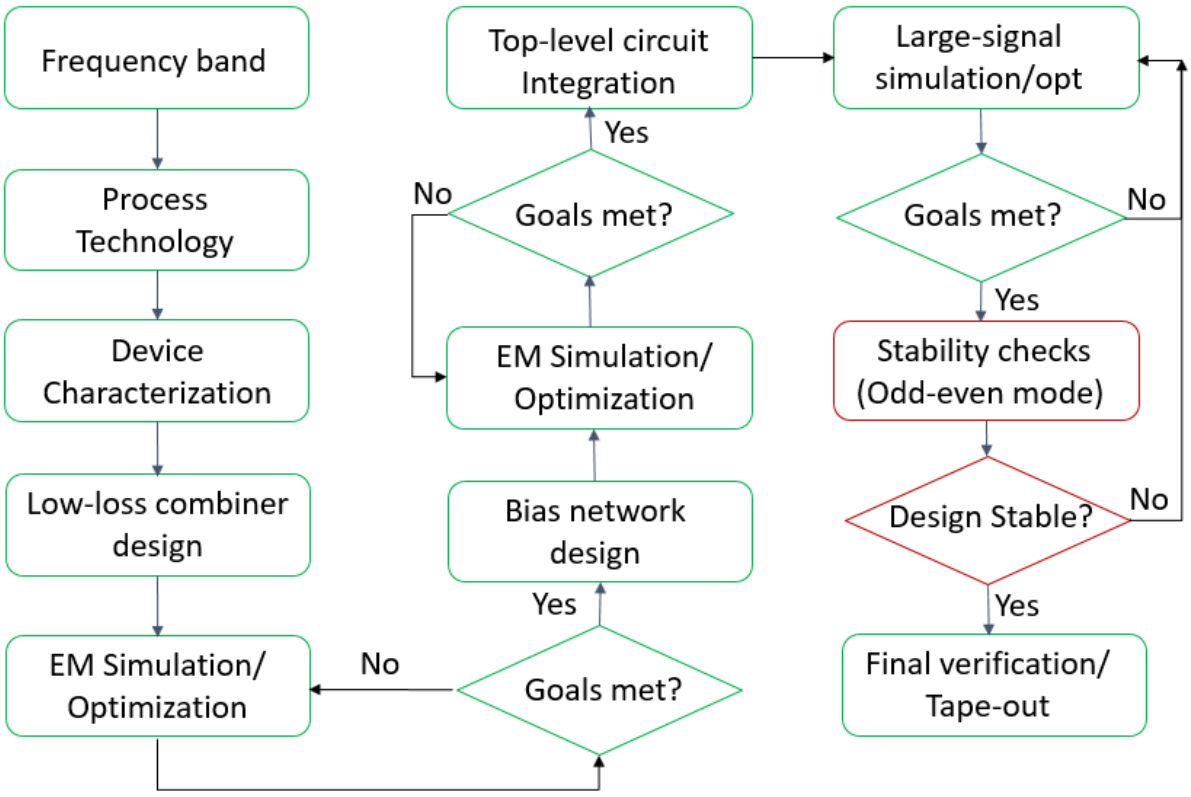

Figure 12: Updated MMIC PA design flowchart with stability checks added

This flow is used in the design of power amplifier which are now fabricated and measured. The measurement results show a good agreement with the models and the design procedure as described earlier. A special care needs to be taken care in performing in small signal and large signal stability analysis.

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2.10 ESR11: Channel emulation platform for system testing mm-wave mobile user scenarios

Note: The author of this section has joined the project in August 2021, and is therefore on a different schedule than the other ESRs. This deliverable reflects the status at the time of writing

Attributed to their short wavelength, the propagation mechanism at mm-waves is different from microwave frequencies. Higher path loss, atmospheric attenuation, rain-induced fading, foliage attenuation, material penetration loss, and ease of blockage are some of the propagation challenges when migrating to the higher frequencies [1], [2]. Consequently, the electromagnetic waves will undergo less diffraction and attenuate severely which will result in a sparse multipath channel with spatial dependencies. This behavior can be emulated in the reverberation chamber by placing absorbers within and covering some parts of its walls [3], [4]. Then, the emulated channel should be assessed using the proposed channel models in literature as discussed in details in D2.2. To facilitate further the assessment process, semi-deterministic model will be used to benefit both from accuracy of deterministic models and simplicity of stochastics counterparts [5], [6]. In this case, the large-scale parameters will be determined using ray tracing and small-scale parameters will be extracted from measurement campaigns.

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2.11 ESR12: Multi-physics modelling for improving design-time and energy-efficiency of highly integrated active antenna arrays

It is now obvious that to meet the current requirements of 5G and beyond system, the hardware implementation of MIMO architectures requires new mmWave packaging and 3D heterogeneous system-integration (stacked integrated circuits (ICs)) platforms as shown in Figure 13. These kind of structures with copper posts or pillars stacked between chip will become common in modern communication systems. However, this system integration has multi-physics aspects, electro-magnetic(EM), thermal, mechanical, etc. High temperature variations may result in the change of EM and thermal properties of the materials which might lead to the generation of electro-thermal passive intermodulation (ET-PIM) due to electrothermal interaction thus impacts the overall system performance. Thermal management is also a big issue in such kind of structure and is necessary from the IC design stages to packages to boards to reduce the thermal resistances in the structure. By predicting thermal and electrical properties in these complex systems can help us to avoid excessive heating and to have a better understanding of the performance of communication systems.

The problems pertaining to generation, detection, and mitigation of PIM and the heat transfer management issue are of great interest to our project partners at Ericsson and we have acquired expertise in such modelling problems over the past years, especially as regards of domain decomposition technique called Linear Embedding via Green's operators (LEGO) for EM fields. Further, ET-PIM has not been investigated for technologies involving posts. Hence, we have selected ET-PIM modelling for configurations with posts, and development of LEGO like technique for thermal modelling for the design evaluation.

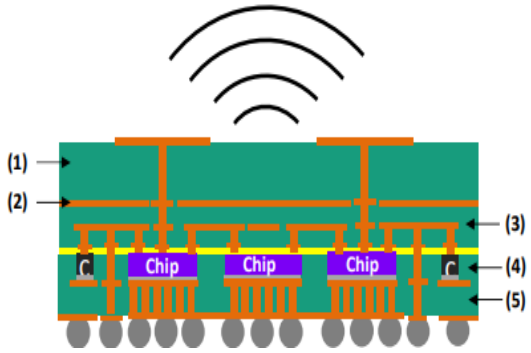

Figure 13: Example of AiP for 5G mmWave 1) antenna layer; (2) shielding layer; (3) re-distribution/routing layer; (4) component layer; (5) temperature control layer [1]

2.11.1 Design evaluation for ET-PIM

I started a preliminary investigation to see whether PIM is a relevant aspect with these modern hardware structures or not in future 5G and 5G+. For that, a paper proposed by [2] is made a basis to develop a simple analytical model where the idea is that the PIM is distributed over an entire cylindrical-via connected through a parallel-plate waveguide. This model analysis of distributed PIM over the entire cylinder is an easier approach than localized PIM, as it makes the problem 2D rather than 3D and thus makes my life much easier to start with the initial simple model. This is the first simplified analytical model to access the level and behaviour of PIM to be expected in such an environment. If the level of PIM is of concern the next step will be to go for localised PIM which is computationally more intensive (3D in nature). Finally, if these simulations indicate possibly significant PIM, more complicated structures between parallel plates can be considered.

2.11.2 Design evaluation for LEGO-like technique

The abbreviation "LEGO" reflects the modular building principle of the method that is common to the well-known LEGO^{TM} bricks. It is a modelling technique developed by the EM group of TU/e to compute EM fields of an individual domain using coupled integral equations. The main idea behind it is that since the current LEGO model computes the electromagnetic field for each of the building blocks, we can make use of the existing model and modify it to compute temperature distribution in each building blocks using steady-state temperature analysis. For that we will apply the integral equation on the heat generated in each of the building blocks to make it boundary value problem and then will connect that in the LEGO fashion but for a scalar problem, rather than time vectorial electromagnetic problem. The electro-thermal coupling, which accounts to nonlinear quadratic coupling can be treated using Karhunen Loève Decomposition.

Note

ET-PIM modelling is my current full attention, and LEGO-like technique will be the next thing depending on what comes out of ET-PIM modelling. If ET-PIM modelling is very promising then we may reduce our effort in the LEGO-like technique and if ET-PIM modelling is not successful and we come to the conclusion that it is not feasible to take it further then we go for LEGO-like technique.

2.11.3 Best Practice Cook Book

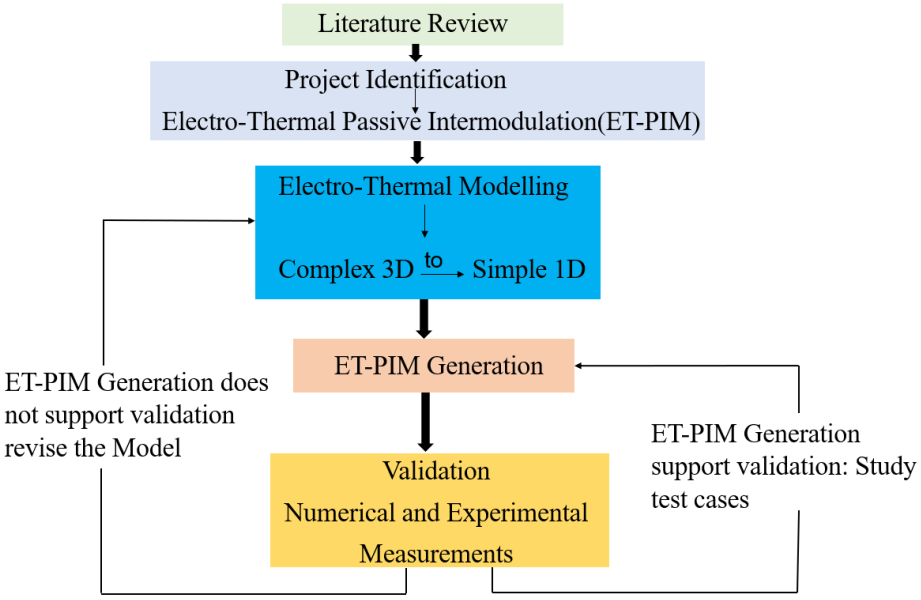

Figure 14: Flow chart summarizing the steps for the best practice cook book for P12 project

Literature Review - The main goal of this project is to develop a method or modelling framework that will support a number of multi-physics phenomena associated with electro-thermo-mechanical design for the development of 5G systems and that will be capable of simulating multi-physics phenomena accurately and efficiently. Initially we identified several potential directions, that have been a topic of research related to modern communication system. Currently, PIM (passive intermodulation) modelling [2],[3] seems to be most relevant candidate, as it directly impacts the system performance. PIM is a phenomenon associated with the generation and propagation of spurious signals (passive intermodulation products) in passive components that is created by mixing that occurs by the nonlinear behavior of components. This nonlinearity can be due to a nonlinear medium (e.g. ferromagnetic materials such as ferrite, Nickel etc.), nonlinear contact (arises due to dirty contacts, metal-metal contact, material defects and metal-insulator-metal contact) and nonlinear interaction that arises from multi-physics due to thermal and electrical signal interaction. It should be noted here that the multi-physics mechanism of the PIM phenomenon is still not very well understood and thus opens the way for us to model it correctly and accurately using best available numerical framework.

ET-PIM - In this project, we proposed a simple parallel plate waveguide model in which a conducting via(resistive material) is sandwiched between two parallel plates. And, the plane wave excitation is made in TEM mode. An analytic formulation of electro-thermally induced non-linearity is then developed for this model. After that using the analytical model derived by [4] for

the calculation of ET-PIM 3 is done. The initial approximate estimation of the results using analytical and numerical method reveals that there is some significant level of ET-PIM3 is produced which decreases with increase in frequency. (This is so far the hypothesis and need to be validated)

Purpose of project – The hardware implementation of MIMO architectures requires new mmWave packaging and 3D heterogeneous system-integration (stacked integrated circuits (ICs)) platforms as shown in Figure 15. These kind of structures with copper posts or pillars stacked between layers are very common in modern communication systems. This system integration however has multi-physics aspects, electro-magnetic(EM), thermal, mechanical, etc. The high power requirements produces high temperature variations that may results in the changes in the resistances which vary with time, the period of which depends on the thermal time constant of device. We know that the power envelope of a signal contains baseband frequency components. If the period of these signals is comparable to the thermal time constant (computed by thermal resistance, (R_{th}) and thermal capacitance, (C_{th})) of the device then intermodulation distortion is generated due to the self-heating of resistive material.

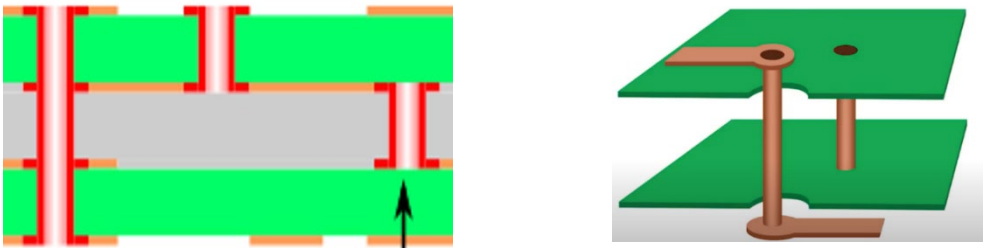

Figure 15: Example of a metallic layer of a PCB connected internally through a copper vias (left) and trans vias connecting microstrip transmission lines(right) [5]

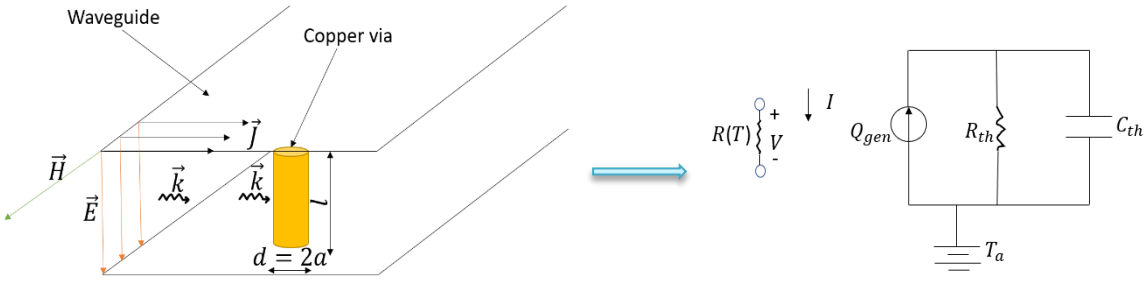

Figure 16: Geometry of the proposed model (left) and simplified model for the generation of Electro-thermal passive intermodulation (right)

Scope of project- In this work a simple analytical model for the estimation of electrothermal passive intermodulation has been proposed. The method extends the idea of electrothermal nonlinearity associated with self-heating of resistive element by high power modulated and multi-carrier RF signals present in the system [6].

Method - In this model, it is assumed that PIM is distributed over cylindrical via of diameter, $d = 2a$ and length, l connected through two parallel plate waveguides, and a plane wave excitation is made in a TEM mode as shown in the Figure 16. The incidence of these plane waves on copper via generates an electric field and hence an electric current. The joule heating due to the finite conductivity of the copper via raises the temperature of the material which changes the resistivity of the material and hence the electric current.

In order to determine how the field penetration into the conductor is affected by an increase in temperature, and how the temperature depends on that field penetration, requires accurate electromagnetic and thermal modelling.

Electromagnetic Modelling - In the electromagnetic modelling we assume that the boundary condition, incidence field, total field, scatter field, and current is constant along z-direction. So,

the problem can be modeled as a 2D plane wave scattering by finite conducting infinite circular cylinder in TEM mode as shown in Figure 17.

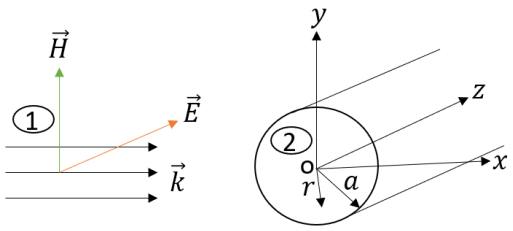

Figure 17: E-polarized plane wave incident on a circular cylinder of finite conductivity

Thermal Modelling – Here we assumed that skin depth is independent of temperature change. We have applied Neuman boundary condition (adiabatic condition) at the outer surface and Robin boundary condition at the center that involves heat transfer coefficient (convection + radiation) as shown in Figure 18. Another assumption here we have made is that since the axial thickness of copper via is small as compared to radial thickness (or length of the via) therefore heat will diffuse in the 1D radial direction due to low radial thermal resistance as compared to axial thermal resistance. So, our problem can be further simplified as a 1D radial heat diffusion problem as shown in the Figure 19. The analytical solution based on the Green's function of [7] for the 1D-radial differential equation governing heat diffusion in the hollow conducting via is obtained.

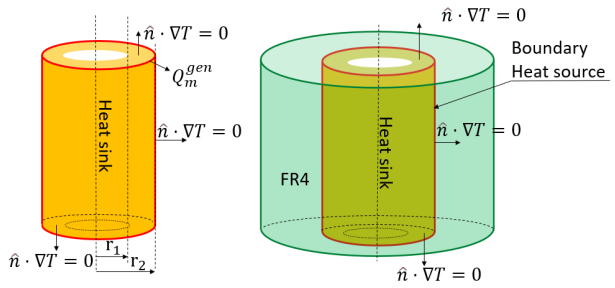

Figure 18: Thermal model for temperature analysis.

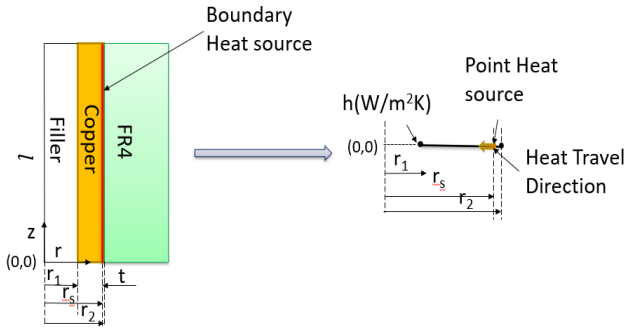

Figure 19: Simplified Thermal model for temperature analysis.

Electro-Thermal coupling - The temperature coefficient of resistance (TCR) is the coupling equation between the two domains, and could be any order polynomial, but is generally described by linear thermo-resistance [8] as $R = R_0\big(1 + \alpha_1(T(t) + T_a)\big)$, where, R_0 is the reference resistance measured at ambient condition, T_a is the ambient temperature, and α_1 is the first order thermo-resistance coefficient.

Electro-Thermal Non-linearity and ET-PIM – Third order ET-PIM in terms of volt is obtained by analytical method proposed by [4].

Validation - Generated PIM is then validated by using numerical method (COMSOL) and experimental measurements.

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2.12 ESR13: Energy efficient signal processing techniques DM-MIMO systems

In this project, strategies will be developed that make efficient communication possible for the distributed massive MIMO networks (also known as cell-free networks). Cell-free massive MIMO is a type of distributed antenna system where a large number of access points (APs) are deployed at different positions in the service area. Each AP can have single or several antennas. In the uplink, each AP simply processes the received signal and then delivers it to a central processing unit (CPU) using the fronthaul links. Afterwards, the CPU recovers transmitted data from different users given the information provided by APs. Cell-free massive MIMO is able to gain diversity against pathloss and can provide uniformly good performance for all the users in the network.

Cell-free massive MIMO systems have advantages such as reduced pathloss and the possibility of some pilot re-use with respect to the collocated massive MIMO systems. However, in the former, the high capacity of the fronthaul links is a limiting factor. High capacitated fronthaul links are required to transmit the digitized signals between the APs and the CPU which demands much more bandwidth than the total user data load.

Besides the general form of cell-free implementation (star topology), radio stripe architecture was proposed for dense scenarios, e.g., stadiums, stations and malls, by Ericsson in Mobile Congress 2019. In radio stripes, multiple APs share one fronthaul cable for synchronization, data transmission and power supply. Here, the capacity of the fronthaul links is still a limiting factor for the total achievable rate of the network. The APs located in each of the stripes form a line network (cascaded network). These line networks can also be seen between some of the APs and the CPU in the general form of the cell-free massive MIMO network.

The investigation of the fundamental limits of these cell-free networks is not sufficiently addressed in the literature. Our goal here is to investigate the fundamental limits of these cascaded networks to develop insight into the capacity of such systems and then translate it into signal processing and coding approaches for cell-free massive MIMO systems. This capacity analysis can be exploited to implement practical signal processing and coding schemes. The state-of-the-art flow chart of this project is shown in the figure below.

It is worth mentioning that performance of these distributed networks could be enhanced by employing power control and AP selection algorithms.

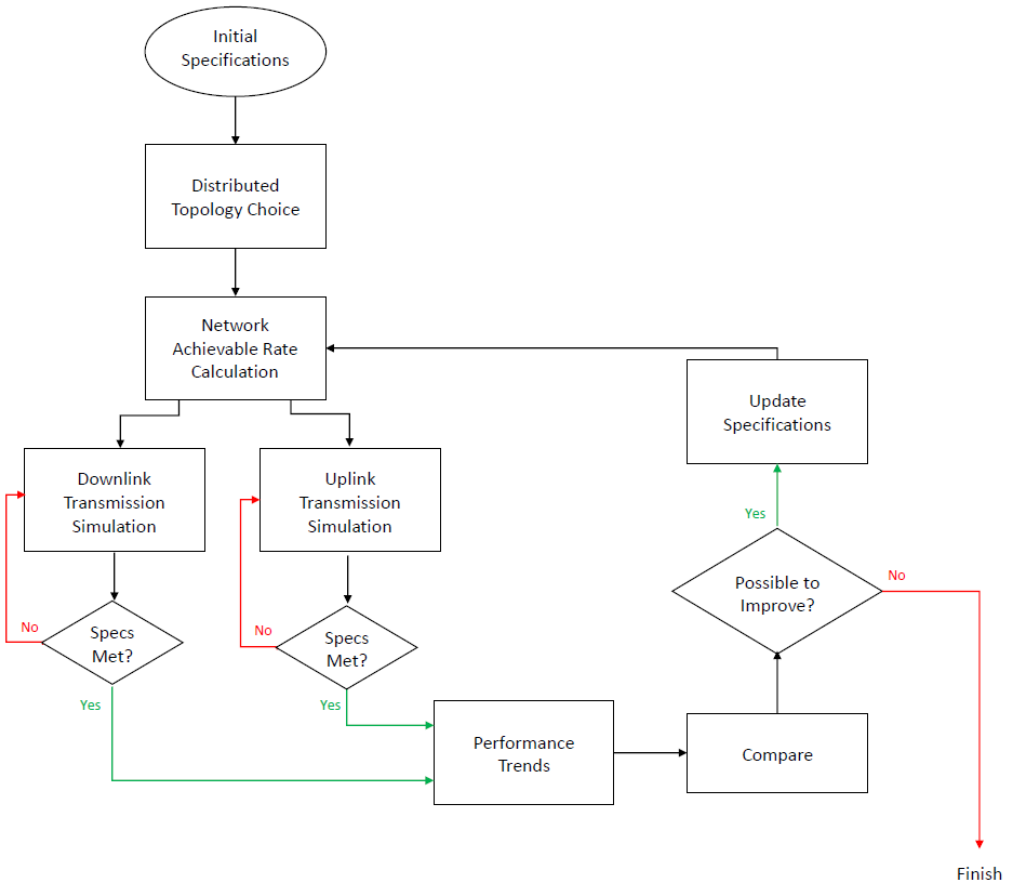

Figure 20: State-of-the-art design flow for project P13.

2.13 ESR14: Digital array calibration techniques and synchronization for DM-MIMO

Any practical communication system consists of several components that play a specific role in transmitting the data stream from one point to another. Oscillators are one of the main building blocks in a communication system. Their role is to create stable reference signals for frequency and timing synchronization. RF oscillators are used to upconvert/downconvert the baseband signal to/from the RF signal (or intermediate frequency signal). Unfortunately, any actual oscillator suffers from hardware imperfections introducing phase noise to the communication system. The fundamental source of the phase noise is the inherent noise of the passive and active components (e.g., thermal noise) inside the oscillator circuitry. The flowchart in Figure 21explains the procedure of this project that shows the effect of synchronization and calibration in our system model as a critical step in this project.

In the context of an uplink-pilot/downlink-precoded transmission cycle, each AP individually processes the observed uplink pilots transmitted by UEs through a synchronization block. Each AP estimates the uplink channel and communicates this to the CP through a digital backhaul network. The CP is, therefore, able to calculate the DM-MIMO precoding matrix. In the downlink transmission phase, the precoded signal at each AP is calibrated. The calibration step compensates for the mismatches caused by the transmitter and receiver AP hardware, such as the non-reciprocal amplitude scaling and phase rotations. On the same time-frequency slot, all the APs in the DM-MIMO network send data simultaneously.

Synchronization is performed for uplink and downlink operations. The synchronization block in the AP synchronizes the frame and carrier frequency to transmit and receive on the assigned time slots. Jointly precoded APs send downlink data that passes the synchronization block to the UEs simultaneously. In this AP block, some signal processing algorithms compensate the timing misalignment and the relative phase rotation of the downlink signal. These algorithms estimate the received signal parameters affected by a timing offset and carrier frequency offset to compensate them.

Calibration compensates for the difference between uplink and downlink RF front-end components. In centralized massive MIMO, antennas are placed near each other, and additional circuits can provide the reciprocity calibration. But there are two methods for reciprocity calibration in distributed massive-MIMO: full calibration and partial calibration.

- In full calibration, an AP can determine its own mismatch matrix and the UE mismatch matrix using the downlink CSI feedback from the UE.
- In partial calibration, only the AP mismatch matrix is determined to achieve multi-user interference suppression. The UE mismatch matrix effect is considered negligible due to its little impact on functional systems performance. This calibration method can be planned besides synchronization.

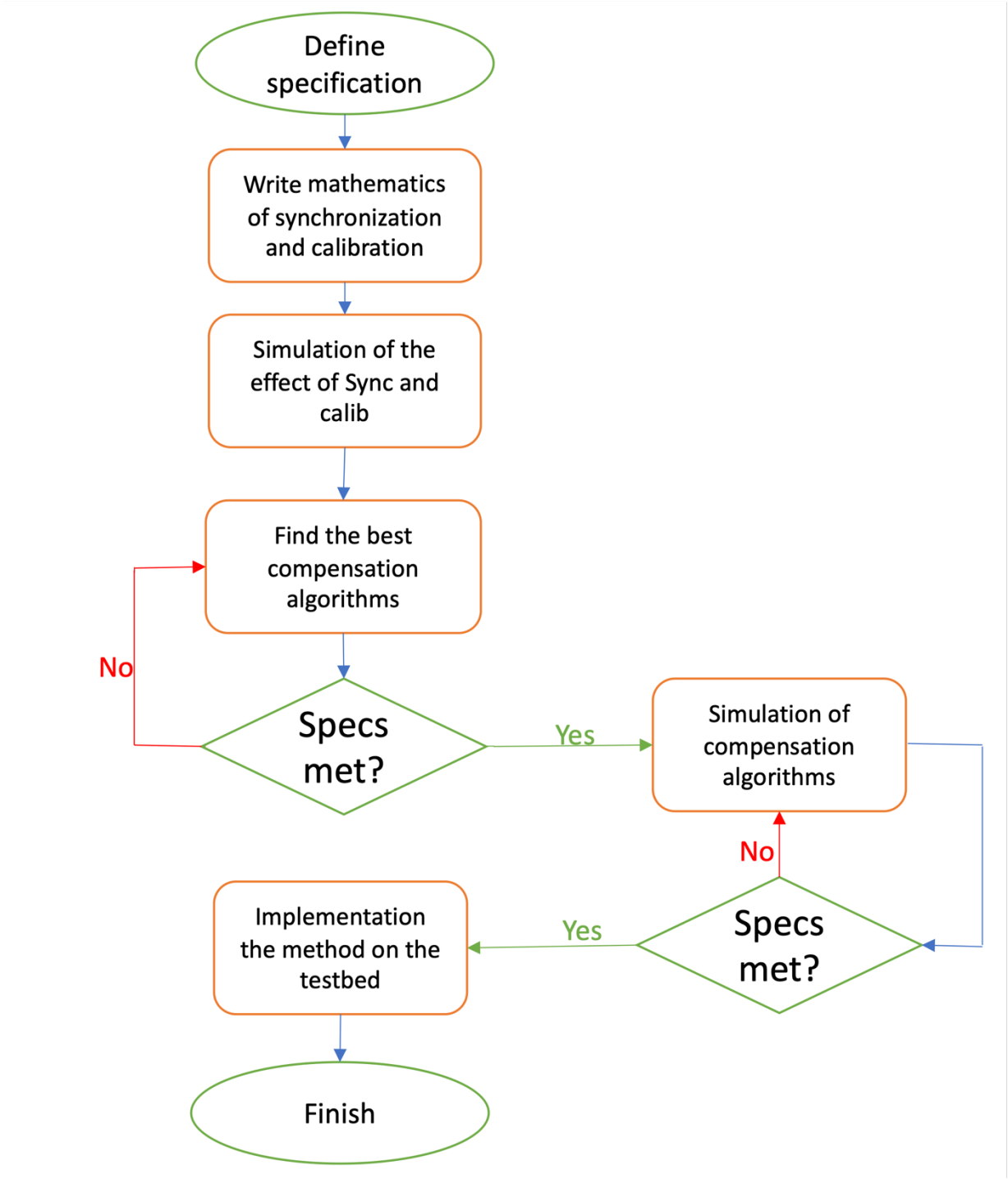

Figure 21: Design flow for project P14

2.14 ESR15: Digital Radio-over-Fiber for flexible mm-wave D-MIMO systems

The design Flow for P15 is Figure 22, which includes software design flow and hardware design flow. The software design flow is responsible for the transmitter/receiver function, followed by co-simulation and co-verification. The transmitter function generates signals from baseband signal through MIMO precoding and sigma-delta modulation, while the receiver function does frequency/timing/phase synchronization for channel estimation with demodulation. All these functions are implemented for the testbed system for an actual demonstration.

The hardware design flow covers digital board, analog board, and antenna design. The digital printed circuit board (PCB) is an off-the-shelf board and requires MATLAB/HDL/Tcl script developments for data transfer and high-speed serial interface of fiber connection. The analog board is a customized PCB for target frequency and starts from schematic/layout design to fabrication with assembly. The antenna is simulated in CST Microwave Studio and designed for millimeter wave frequency. The antenna dimensions correspond approximately to half a wavelength at the center frequency.

At the system integration, a SISO system demonstration is implemented at first. The system verification includes power level measurements and bandwidth sweeps at each stage. A laboratory equipment, a vector signal analyzer from Keysight, works as a receiver for over-the-air demonstration. Multiple distributed transmitters are also integrated and demonstrated later. Two receiving antennas are two users for MIMO demonstration to show the feasibility and performance of the MIMO system. The distributed fiber link coherence is important to check, and the MIMO precoding algorithm is a Zero-Forcing method during the demonstration.

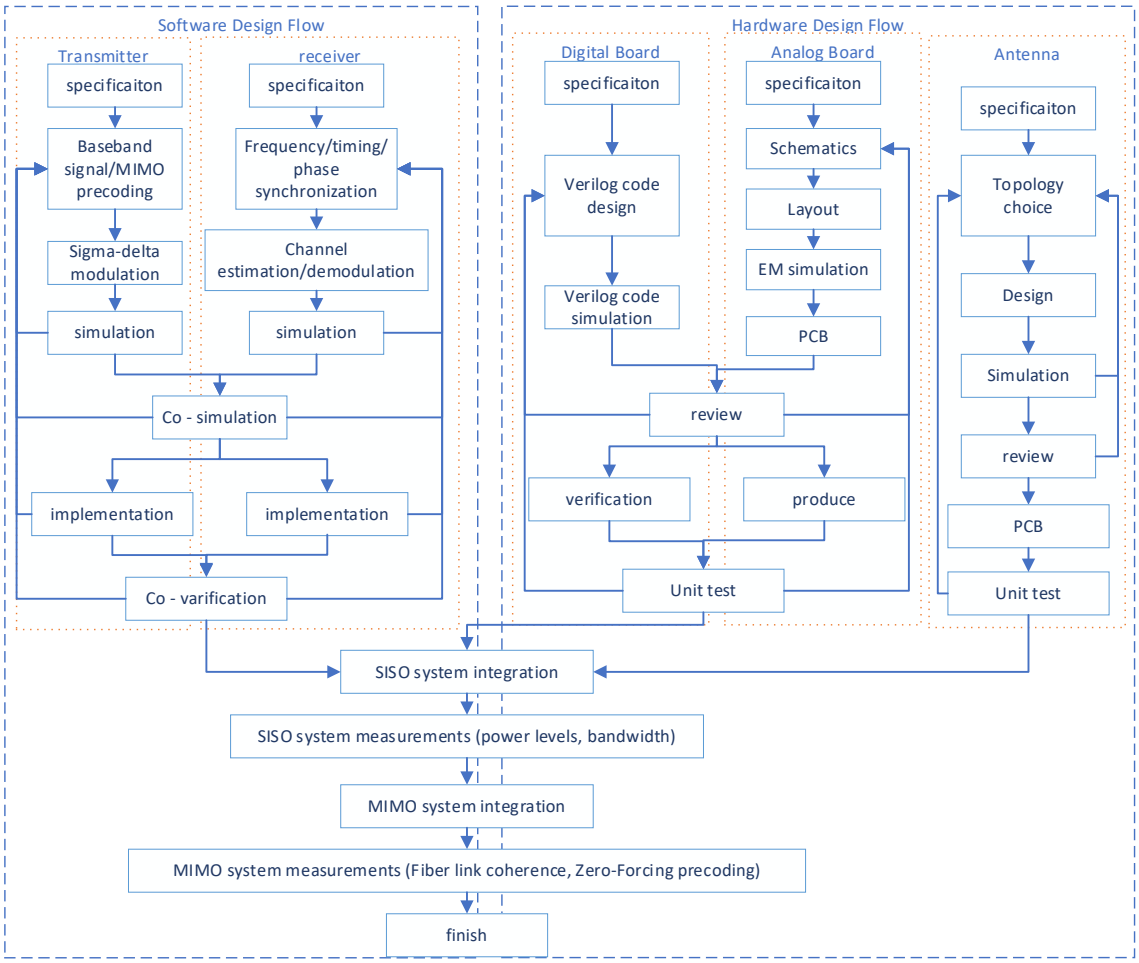

Figure 22: Design flow for P15

Table 3 Software and equipment requirements for the design

Requirement	Description	Version
ADS	For hardware design	The latest version
CST	For antenna design	The latest version
Matlab	For signal processing algorithm development	The latest version
Vivado	Digital board developments	The latest version
Signal generator	In verification step, need it to verify design	The more features the better
Spectrum analyzer	To determine signal quality	Need to cover 500 MHz bandwidth at least
Oscilloscope	To see real time signal in time domain and for fiber link coherence	Need 20 Gsps sample rate at least

3 Conclusions

The design flows used have been suggested and improved significantly since the establishment of the state-of-the-art in the previous documents D2.1 to D2.3.

14 ESR have progressed in their individual projects after 28 months.

The individual findings from the 14 working PhD are significant in the following areas:

- Comprehensive and Multiphysics-based integration of antennae
- Efficient MMIC design for PA and LNA at various frequencies
- Active Antenna control
- Testing
- Frequency expansion beyond 100 GHz
- Signal processing and calibration
- Electro-optical interaction

With these achievements the project Mywave comes to a significant conclusion in advanced education, design, and hardware progress.